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Heat sink efficiency investigation of silicon-on-diamond composite substrates for gallium nitride-based devices

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In this work, thermometric measurements of gallium nitride-based ungated transistors on silicon-on-diamond composite substrates are performed. Their heat sink efficiency is compared with transistors made by standard technology on a silicon carbide substrates. Reducing of the surface temperature by more than 50°C using new type of silicon-on-diamond composite substrates at dissipation power above 7 W is shown. The proposed approach is promising for increasing the output power and reliability of gallium nitride-based devices.

Keywords: gallium nitride, heat sink, diamond, dissipation power.

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Gallium nitride (GaN) heterostructures are used efficiently in communication devices, radars, and secondary energy converters [1]. High values of the specific current density and the breakdown voltage provide an opportunity to fabricate GaN elements with a specific output power exceeding 5 W/mm [2]. However, since the thermal conductivity of silicon and silicon carbide (SiC) substrates used to fabricate epitaxial heterostructures is relatively low, the active region of transistors is heated significantly. The self-heating of structures limits the output power potential and reduces the mean time before failure (MTBF). Diamond has a record-high thermal conductivity for a bulk material. The thermal conductivity coefficient of polycrystalline diamond films grown by microwave plasma-enhanced chemical vapor deposition is as high as $800-1800\,\mathrm{W/(m\cdot K)}$ [3]. Therefore, diamond is a promising material for the construction of an efficient heat sink for the active region of GaN transistors.

Several methods for integration of gallium nitride heterostructures with a diamond heat sink (GaN-on-diamond) have already been demonstrated [4–6]. However, no meaningful progress in reducing the temperature of the active region of transistors has been made yet. This hinders the introduction of GaN-on-diamond technology into the process of fabrication of high-power microwave devices.

We have demonstrated an original scalable approach to integration of GaN heterostructures with a diamond heat sink for the first time in [7,8]. Device-quality GaN heterostructures were produced in these studies on substrates 15×15 mm in size, transistors were fabricated based on them, and their static characteristics were examined.

In the present study, the surface temperature of interdigitated structures is examined with the purpose of estimating the heat-sink efficiency of composite GaN-on-diamond substrates, and the obtained results are compared to the standard GaN-on-SiC technology.

Commercially available GaN-on-SiC transistors with a source–drain distance of $4\,\mu$m, a period of $25\,\mu$m, a gate length of $0.2\,\mu$m, and a total gate periphery of 1.25 mm (TGF2023-2-01, Qorvo, United States) were used as reference samples. The gate was shorted to the transistor source in advance to exclude the influence of floating-gate effects. Topological equivalents of interdigitated GaN-on-diamond structures were fabricated to make a correct comparison.

The technology of fabrication of composite GaN-on-diamond substrates was detailed in [7]. Transistor crystals were mounted in a ceramic-and-metal package of a power transistor. The method of soldering with a eutectic Au80/Sn20 alloy was chosen to minimize the crystal–package thermal resistance. A piece of 25-μm-thick foil made from this alloy was used. The base of the transistor package was a 2.5-mm-thick plate made from a Cu–W pseudoalloy. This plate was coated with an electrodeposited gold layer with a thickness of about $5\,\mu$m. The device package with crystals was mounted on a bulk copper heat sink; thermal paste was applied to improve the quality of thermal contact. The bonding of internal leads of microwave transistors was performed using an F&K Delvotec 5630 setup with a gold wire $25.4\,\mu$m in diameter.

Dependences of the surface temperature on the dissipated power were measured in the DC mode using a QFI InfraScope temperature mapping microscope. Temperature changes were recorded with a MWIR camera that was cooled by liquid nitrogen and operated at a wavelength of $1-5\,\mu$m. The sizes of the intensity map (1000×1000 pixels) and the field of view ($750\times750\,\mu$m) yield a resolution of about $0.75\,\mu$m per pixel. The setup was fitted with a temperature-stabilized table with an operating temperature range of 10–140°C. The sensitivity of the instrument was 0.1°C.

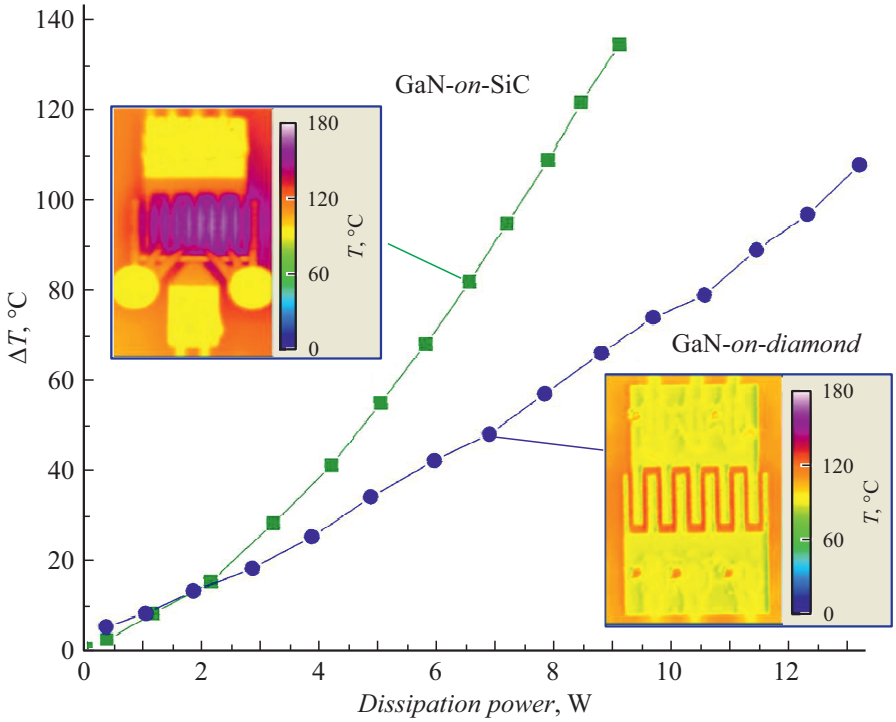

Figure 1. Dependence of increment ΔT of the maximum temperature in the active region of a transistor relative to the base temperature on the dissipated power for GaN-on-SiC and GaN-on-diamond transistor structures. The maps of temperature distribution in GaN-on-SiC and GaN-on-diamond transistor structures at a dissipated power of 6.6 W are shown in the insets.

Measurements were performed at a base temperature of 85°C, which is the reference point for device operation in such conditions when only external air cooling is available.

The current–voltage curves (CVCs) were measured using a Cascade PM5 probing system with a Keithley 2636B dual-channel sourcemeter.

Figure 1 presents the dependence of increment ΔT of the maximum temperature in the active region of a transistor relative to the base temperature on the dissipated power.

Manufacturers of discrete GaN-on-SiC transistors advise against such operation modes where the channel temperature exceeds 200°C, since this reduces the MTBF significantly. Specifically, the manufacturer of the reference transistor specifies that its surface temperature should not exceed 184°C at a maximum recommended dissipated power of 6.25 W in the DC mode. This corresponds to $\Delta T = 99$°C and matches the result presented in Fig. 1. At a dissipated power of 8.5 W, temperature increment ΔT for the structure on SiC is already higher than 120°C, while ΔT for the structure on diamond is below 70°C. This temperature difference of crystals translates into an MTBF difference of two orders of magnitude [9]. At the same time, $\Delta T = 115$°C, which corresponds to a channel temperature of 200°C, for structures on diamond is achieved at a dissipated power in excess of 13 W. Figure 1 also shows the temperature distribution maps (see insets) obtained at a dissipated power of 6.6 W, which corresponds to a specific power of ~ 5 W/mm typical of modern devices. The maximum temperature in the working region of the channel of the transistor on SiC was 172°C. This corresponds to an MTBF below 10^9 h. The maximum temperature in the working region of the channel for the structure on diamond was 133°C. With the MTBF research data factored in, transistors based on GaN-on-diamond have the potential to provide more than 10^{11} h of stable operation in this mode [9].

Thus, the proposed diamond heat sink technology allows one to increase the mean time before failure or the dissipated power without increasing the temperature of transistor channels. It provides an opportunity to reduce the area of the active transistor region while keeping the total gate width unchanged.

Figure 2 shows the measured CVCs of structures. The maximum drain current density for GaN-on-SiC transistors and GaN-on-diamond interdigitated structures was 0.82 and 0.88 A/mm, respectively. It can be seen that the drain current of GaN-on-SiC transistors decreases at voltages above 6 V due to self-heating, while no self-heating was observed for GaN-on-diamond interdigitated structures within the entire measurement range. Thus, GaN-on-diamond structures provide an opportunity to raise the dissipated power by 37% at a supply voltage of 15 V.

We note in conclusion that the results of thermometric measurements performed for interdigitated structures on silicon-on-diamond composite substrates reveal a considerable surface temperature reduction with respect to SiC. This

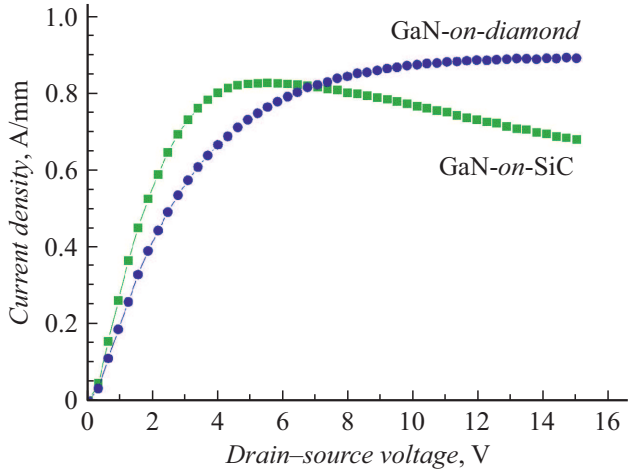

Figure 2. Current–voltage curves of GaN-on-SiC transistors and GaN-on-diamond interdigitated structures.

allows one to increase the MTBF by a factor of 100 (or more) by reducing the channel temperature by over 50°C at a dissipated power above 7 W. It was demonstrated that GaN-on-diamond structures do not manifest any effects of self-heating in CVC measurements up to 15 V. This provides an opportunity to raise the dissipated power by 37% (relative to commercially available GaN-on-SiC transistors).

Owing to the suppression of self-heating by efficient heat abstraction, the developed approach opens up new possibilities for further progress in GaN technology.

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Conflict of interest

The authors declare that they have no conflict of interest.

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