Electrical properties of MOS capacitors formed by PEALD grown Al_2O_3 on silicon

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In the present work, we have grown 2.83 nm thin Al_2O_3 films directly on pre-cleaned p-Si(100) substrate using precursor Trimethyl Aluminium (TMA) with substrate temperature of 300°C in a Plasma Enhanced Atomic Layer Deposition (PEALD) chamber. The MOS capacitors were fabricated by depositing Pt/Ti metal bilayer through shadow mask on Al_2O_3 high-k by electron beam evaporation system. The MOS devices were characterized to evaluate the electrical properties using a capacitance voltage (CV) set-up. The dielectric constant calculated through the CV analysis is 8.32 for Al_2O_3 resulting in the equivalent oxide thickness (EOT) of 1.33 nm. The flat-band shift of 0.3 V is observed in the CV curve. This slight positive shift in flat-band voltage is due to the presence of some negative trap charges in Pt/Ti/ALD$-Al_2O_3$/p-Si MOS capacitor. The low leakage current density of $3.08 \cdot 10^{-10}$ A/cm^2 is observed in the JV curve at 1 V. The Si/Al_2O_3 barrier height Φ_B and the value of J_{FN} are calculated to be 2.78 eV and $3.4 \cdot 10^{-5}$ A/cm^2 respectively.

1. INTRODUCTION

The Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) are the basic building blocks of the current ULSI circuits. The processing speed and electrical power dissipation which are dependent on the geometrical size of MOSFET decides performance of silicon ULSI devices. The miniaturization of the metal oxide semiconductor (MOS) devices following the Moore's law has lead to the extreme thinning of the commonly used SiO_2 gate oxide. However, this thinning has reached its limits because of the dramatic increase of the leakage current through the oxide, causing the degradation of the devices [1–4]. In order to find appropriate substitute for insulating SiO_2 the traditional gate oxide in silicon based nanoelectronics MOS devices need the higher-k dielectrics to minimize the EOT (Equivalent Oxide Thickness) for better performance. A variety of high-permittivity metal oxides have been intensely studied during the last decade such as HfO_2, TiO_2, CeO_2, ZrO_2, Al_2O_3, $LaAlO_3$, HfSiO etc [5–6]. Among the properties of high-k oxides, the thermal stability of high-k dielectric on silicon is an important issue for future MOSFET devices. Al_2O_3 exhibits large band gap 7–8 eV high field strength, excellent thermodynamic stability on Si to reduce the tunneling current for the same gate capacitance, dielectric constant of 9 and large band offsets [7–9]. The deposition methods and the deposition conditions tend to determine the crystallinity and purity of deposited dielectric thin films. High temperature annealing can result in the crystallization and densification of dielectric materials. Deposition of high-k layer on Si substrate can be done by variety of techniques such as ALD [10], RF Sputtering [11], MOCVD [12], PLD [13], sol-gel [14,15], PEALD [16] etc. In nanoelectronics, continuous shrinking of devices improves the performance, which sets challenging requirements for the integrated circuit (IC) fabrication. As requirements tighten, the novel thin film deposition techniques are needed in many applications. The current interest in ALD in the nanoelectronics industry stems from the unique characteristics that, this method offers deposition of ultrathin films on a large substrate area with excellent properties and with control of thickness and composition at sub-nanometer level [10]. As the nanoelectronics industry looks to transition to both three dimensional transistor and interconnect technologies at the < 22 nm node, highly conformal dielectric coatings with precise thickness control are increasingly being demanded. Plasma enhanced atomic layer deposition (PEALD) currently plays this role for most of the applications requiring low temperature processing, good step coverage and precise thickness requirements. In PEALD, gases that provide radical atoms or ions for the reaction under the plasma condition are normally inactive with the metal precursors at the process temperature. Thus no deposition can be expected where plasma doesn't exist. The properties of dielectric thin films can be studied by fabricating metal oxide semiconductor structure by depositing suitable metal gates. Candidates for new metallic gates have many requirements which include appropriate work function good thermal and chemical interface stability with underlying dielectric and high carrier concentration and process compatibility with current and future CMOS devices. Metal bi-layered electrode structures of ultrathin layer of low work function metal followed by comparatively thicker layer of high work function metal, like Nb/W, Ti/Pt, Ti/W, Al/TaN etc have been used in recent past for the purpose of forming the better MOS devices through the work function tuning [17]. This work reports the deposition of Al_2O_3 high-k thin film on silicon substrate and fabrication

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of MOS capacitors using Pt/Ti bi-layer metal electrodes. The experimental details are described in the second section of the paper and the third section describes some related theoretical aspects. Results are described in fourth section and fifth section concludes the paper.

2. EXPERIMENTAL

P-type Si(100) substrates were used for the deposition of Al_2O_3 high-k thin films. Substrates were ultrasonically cleaned in Acetone for 2 min at 15°C and methanol for 1 min at 15°C followed by a rinse in deionized (DI) water for organic removal. Samples were then cleaned in buffered Hydrofluoric acid (BHF) for native oxide removal followed by a rinse in DI water. The substrates were then dried and put into the deposition chamber of the PEALD (Model-Oxford FlexAL) system. Trimethyl Aluminium (TMA) and oxygen plasma were used as the precursor materials for the Al_2O_3 deposition at 300°C substrate temperature. The ALD growth cycle consisted of the following steps: 10 ms TMA dose at 20 mT chamber pressure, 2 s of argon purge, 5 s of oxygen plasma at 250 W ICP power and 10 mT chamber pressure. The Pt/Ti metal bilayer electrodes were deposited by electron beam evaporation (CHA model no. SEC-600) through a shadow mask with electrode area of $1.77 \cdot 10^{-4}$ cm^2 to fabricate the MOS capacitors. Ti and Pt have thicknesses of 2 nm and 20 nm at the deposition rate 0.2 Å/s and 0.5 Å/s respectively. Rapid thermal annealing (RTA, AET Model No-RX-6) was performed on the fabricated Pt/Ti/ALD–Al_2O_3/*p*-Si MOS capacitors at 350°C in a forming gas environment ($N_2 : H_2$, 90 : 10) for 30 min. Backside metal contact was formed by depositing the Aluminum using the thermal evaporation system. The deposited films and fabricated MOS capacitor were characterized using a spectroscopic ellipsometer (M2000DI JA Woollam Co-Inc) for film thickness measurement, capacitance-voltage (Agilent 4284A LCR) and current–voltage (semiconductor characterization system 4200) for electrical properties.

3. RESULTS AND DISCUSSION

3.1. Ellipsometry

The thickness of the Al_2O_3 film was found to be 2.83 nm measured using variable angle spectroscopic ellipsometry. The equivalent oxide thickness (EOT) of 1.32 nm has been determined by using physical thickness of Al_2O_3 layer and dielectric constant obtained from the capacitance voltage (*CV*) measurement, which is compatible to the current technology nodes.

3.2. Capacitance–Voltage (*CV*) and Conductance Voltage (*GV*) Measurement

The Pt/Ti/ALD–Al_2O_3/*p*-Si MOS capacitor was characterized by the Agilent 4284A LCR meter for the measurements of dielectric properties of the fabricated MOS structure. A typical *CV* characteristics curve of MOS structure is shown in the fig. 1. The dielectric constant (k) value of sample annealed at different temperatures was extracted from the accumulation level of a *CV* curve and was calculated using the following equation

$$k = (C_{ox} t_{ox})/(\varepsilon_0 A). \quad (1)$$

Where, C_{ox} is the oxide capacitance, t_{ox} is the thickness of oxide layer, ε_0 is the permittivity of free space and A is the electrode area. The dielectric constant determined from accumulation capacitance of *CV* curve obtained at 1 MHz is 8.32. In *CV* curve a slight negative shift is observed in the flat-band voltage because of the presence of positive trap charges (Q_{eff}) in the Al_2O_3 MOS capacitor. The Q_{eff} can be found by using Eq. (2) and thus calculated to be $4.88 \cdot 10^{12}$ cm^{-2} [18]. The frequency dispersion in *CV* curves is observed in figure 1 due to the presence of trap charges. The value of interface trap density (D_{it}) is determined from the *CV* and conductance–voltage (*GV*) curve of Fig. 1 and 2 and calculated from the Hill–Coleman

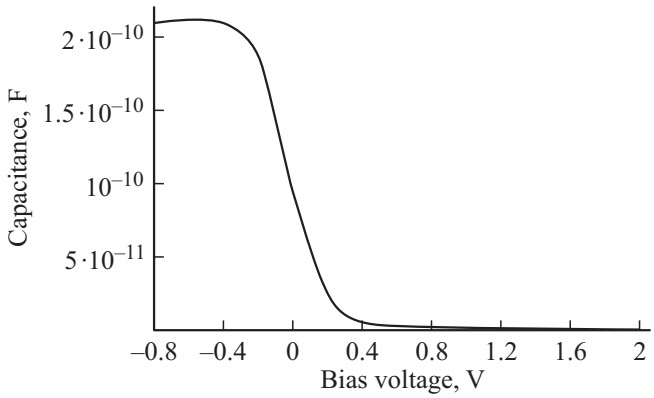

Figure 1. Capacitance-Voltage characteiristics of Pt/Ti/ALD–Al_2O_3/*p*-Si MOS capacitor.

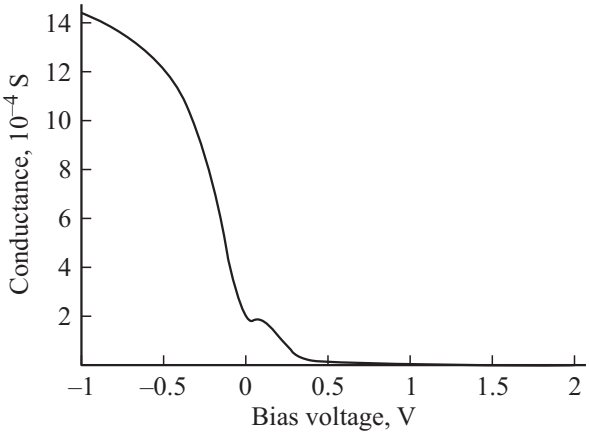

Figure 2. Conductance-Voltage characteiristics of Pt/Ti/ALD–Al_2O_3/*p*-Si MOS capacitor.

method using Eq. (3) [19]:

$$Q_{\text{eff}} = (\Delta V_{\text{FB}} C_{\text{ox}})/qA, \tag{2}$$

$$D_{\text{it}} = \frac{2\omega C_{\text{ox}}^2 G_{\max}}{qA\{G_{\max}^2 + \omega^2[C_{\text{ox}} - C_m(G_{\max})]^2\}}. \tag{3}$$

Where, ΔV_{FB} is the flat band voltage shift, q is electronic charge, C_m is maximum capacitance, $G_{\max}$ is the maximum conductance and ω is frequency. The value of D_{it} for 1 MHz frequency is found to be $1.30 \cdot 10^{13}\,\text{cm}^{-2}\,\text{eV}^{-1}$. The density of interface trap is very high and may be due to poor interface quality at Si/Al_2O_3 due to direct deposition of Al_2O_3 on p-Si substrate.

3.3. Current density–voltage (JV) measurement

Fig. 3 shows the leakage current density–voltage (JV) curve of 2.83 nm thin Al_2O_3 based MOS capacitor having a leakage current density of $3.08 \cdot 10^{-10}\,\text{A/cm}^2$ of forming gas annealed Al_2O_3 at 1 V biasing voltage, indicating good electrical integrity at 1 V biasing voltage.

According to quantum mechanics, the charge carriers tunnel through triangular barrier into the conduction band of an oxide; it is termed as FN tunneling [20–24]. The leakage current density found by FN tunneling, J_{FN}, can be described by

$$J_{\text{FN}} = AE^2 \exp(-B/E), \tag{4}$$

where,

$$A = q^3 m_0/(8\pi h m^* \Phi_B), \tag{5}$$

$$B = 4(2m^*)^{1/2}(q\Phi_B)^{3/2}/(3qh/2\pi), \tag{6}$$

$$J = I/A \tag{7}$$

and

$$E = (V_G + V_{\text{FB}})/EOT, \tag{8}$$

where A is the Richardson constant, q is the electronic charge, h is Planck's constant, m_0 is the free electron mass, m^* is the effective electron mass in oxide, and Φ_B is the barrier height between the p-type Si and gate oxide, V_G is the gate voltage. Fig. 4 shows a plot of J/E^2vs$1/E$ resulting from the data in Fig. 3. The tunneling parameter B is the slope of the linear region in the FN plot [$\ln(J/E^2)$vs$1/E$].

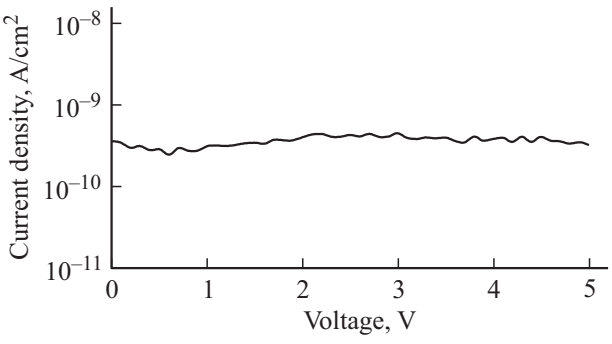

Figure 3. Current density vs voltage (JV) curve of Pt/Ti/ALD–Al_2O_3/p-Si MOS capacitor.

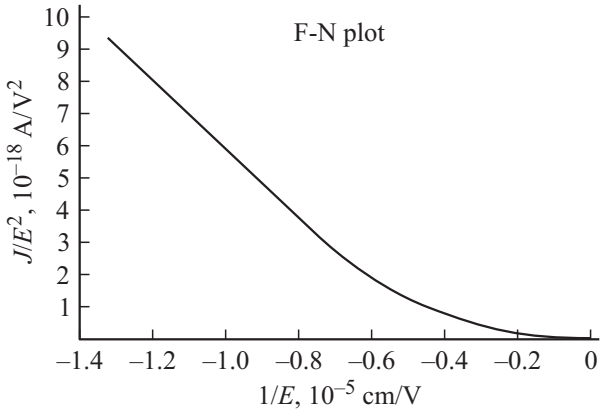

Figure 4. Fowler-Nordheim (FN) plot of Pt/Ti/ALD–Al_2O_3/p-Si MOS capacitor.

The magnitude of this slope can be used to calculate the Si/Al_2O_3 barrier height. E is the oxide electric field derived from the applied potential corrected for the flat-band voltage, $V_{\text{FB}} = 0.3$ V, divided by the film equivalent oxide thickness. The effective mass of an electron in Al_2O_3 is $m^* = 0.35m_0$. Using this effective mass, the Si/Al_2O_3 barrier height Φ_B is calculated as 2.78 eV based on the data in Fig. 4 and the value of J_{FN} is calculated to be $3.4 \cdot 10^{-5}\,\text{A/cm}^2$ at 4 MV/cm.

4. CONCLUSIONS

The Al_2O_3 thin films were successfully deposited with controlled thickness using PEALD technique and the Pt/Ti/ALD–Al_2O_3/p-Si MOS capacitors were fabricated by depositing Ti/Pt bi-layer metal contacts. We have investigated the electric properties like density of interface traps, leakage current density and conduction mechanism which holds good electrical integrity from the CV/IV curves obtained for fabricated MOS capacitors. These values of the electrical characteristics of the fabricated Pt/Ti/ALD–Al_2O_3/p-Si MOS capacitors can be considered to be suitable for current technology nodes.

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