Influence of gate-to-source and gate-to-drain recesses on GaAs camel-like gate field-effect transistors

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In this article, the characteristics of the GaAs homojunction camel-like gate field-effect transistors with and without the gate-to-source and gate-to-drain recesses structures are first investigated and compared. As to the device without the recesses structure, a second channel within the n^+-GaAs cap layer is formed at large gate bias, which could enhance the drain output current and transconductance. Furthermore, a two-stage relationship between drain current (and transconductance) versus gate voltage is observed in the recesses structure. The simulated results exhibit a maximum drain saturation current of 447 (351 mA/mm) and a maximum transconductance of 525 (148 mS/mm) in the studied device without (with) the recesses structure. Consequentially, the demonstration and comparison of the variable structures provide a promise for design in circuit applications.

1. INTRODUCTION

III-V field effect transistors (FETs) have been widely applied on the signal amplifiers and microwave integrated circuits [1–4]. Nevertheless, due to the small gate potential barrier height at metal-semiconductor (M-S) contact in the traditional III-V FETs, it is difficult to achieve high gate turn-on voltage, high output current, and broad gate voltage swing [5]. Previously, the $n^+/p^+/n$ camel-like gate FETs had been realized to overcome the above disadvantage for the employment of a camel-like gate attributed to (i) the high gate potential barrier in accordance with the characteristics requirement to make adjustments by changing the $n^+/p^+/n$ doping concentration and thickness and (ii) the potential for improving reliability at high power condition [5–7]. In the camel-like gate structure, the p^+-layer must be relatively thin and heavily doped to ensure that the layer is completely depleted and camel-like gate depletion can be formed at equilibrium and under gate biases. In the previous reports, it was suggested that gate-to-source (G-S) and gate-to-drain (G-D) region needs to be recessed to avoid gate to other electrodes short [5–7]. However, the effect of the recesses on the device performance has not been investigated until now.

In this article, we first demonstrate the influence of gate-to-source and gate-to-drain recesses on the characteristics of GaAs homojunction camel-like gate FETs. It is found that the device without the recess structure exhibits a larger drain current and a relatively higher transconductance value, which can be attributed that a second channel is formed within the n^+- GaAs cap layer at gate forward bias.

2. DEVICE STRUCTURES

The structure layers consisted of a 3000 Å GaAs undoped buffer layer, a 500 Å $n^+ = 1 \cdot 10^{18}\,\mathrm{cm}^{-3}$ GaAs channel layer, a 100 Å $p^+ = 8 \cdot 10^{18}\,\mathrm{cm}^{-3}$ GaAs layer. Finally, a 200 Å $n^+ = 6 \cdot 10^{18}\,\mathrm{cm}^{-3}$ GaAs cap layer was constructed on the p^+-GaAs layer. The FETs without and with the gate-to-source and gate-to-drain recesses structures are labelled as devices A and B, respectively. The metal was deposited with Au on the n^+-GaAs cap layer. Fig. 1, *a*

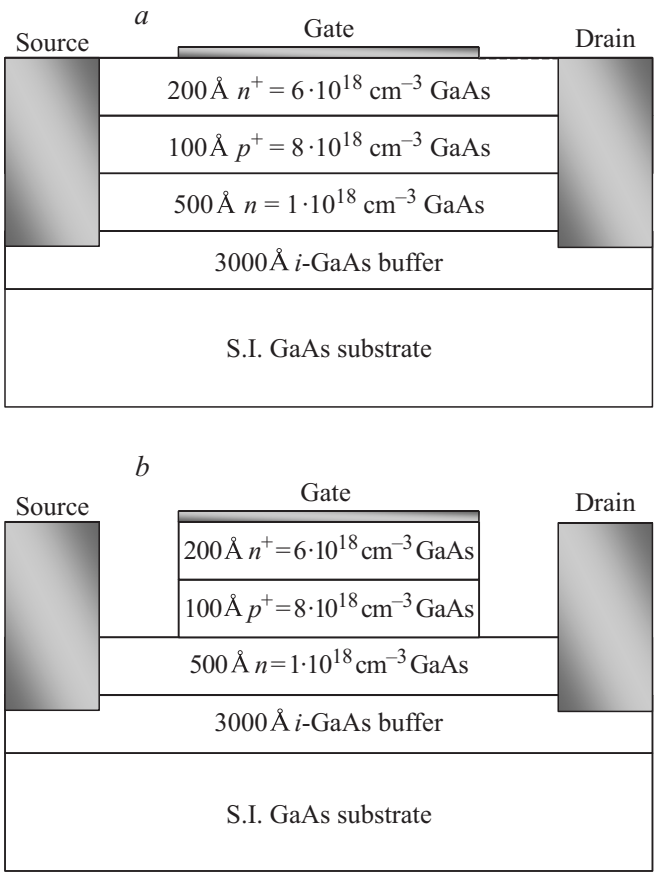

Figure 1. Schematic cross section of the studied devices. Devices A and B represent the FETs without and with the gate-to-source and gate-to-drain recesses, respectively.

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and *b* depict the schematic cross sections of the devices A and B, respectively. In the device B, the n^+-GaAs cap layer and p^+-GaAs layer were recessed within G-D and G-S region. The gate dimension and drain-to-source spacer were $1 \times 100\,\mu m^2$ and $3\,\mu m$, respectively. A two-dimensional semiconductor simulation package SILVACO was employed to analyze the device characteristics [8]. The simulated analysis took into account the Poisson equation, continuity equation of electrons and holes, Shockley–Read–Hall (SRH) recombination, Auger recombination, and Boltzmann statistics, simultaneously.

3. RESULTS AND DISCUSSION

Fig. 2, *a* and *b* shows the common-source current-voltage (*I-V*) characteristics of the devices A and B, respectively. A maximum drain currents of 47.8 and 34.1 mA are observed at $V_{GS} = 1.5\,V$ and $V_{DS} = 10\,V$ for the devices A and B, respectively. When compared to the device B, the device A without the recesses structure exhibits a higher collector current. Nevertheless, obvious gate leakage current is observed at $V_{GS} \geq 1.25\,V$ in the device A. The reason will be explained in detail by the energy band diagram in Fig. 4.

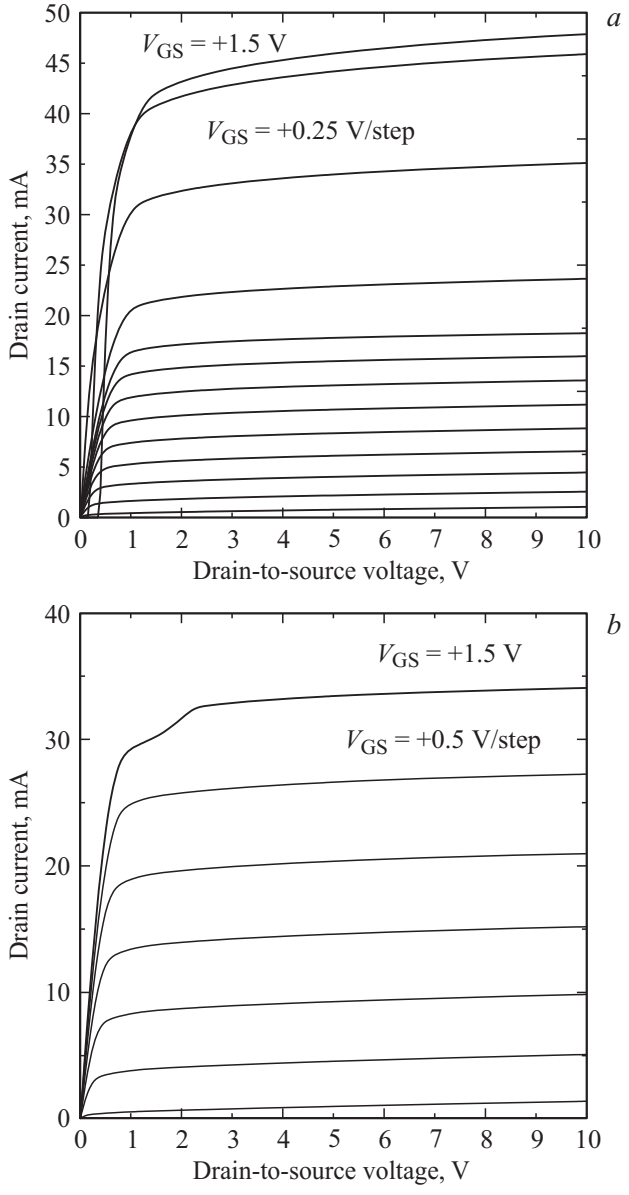

Figure 2. Simulated drain-to-source current-voltage characteristics of the (*a*) device A and (*b*) device B.

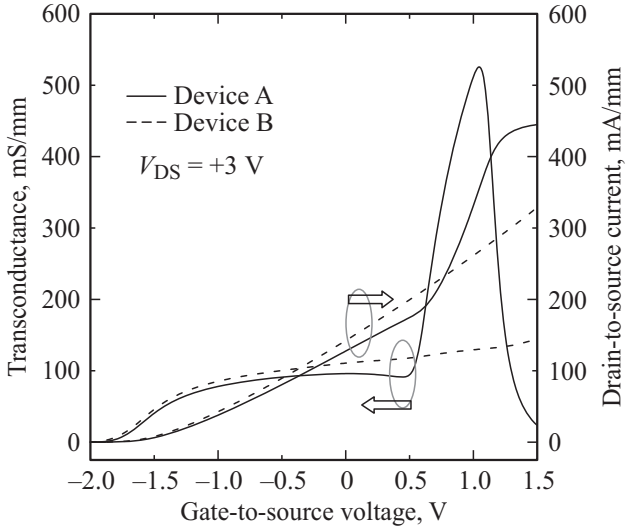

Figure 3. Drain-to-source saturation current and transconductance versus gate voltage at $V_{DS} = +3\,V$.

The drain-to-source saturation current and transconductance versus gate voltage at $V_{DS} = +3\,V$ are illustrated in Fig. 3. In the device A (device B), it exhibits a maximum drain saturation current of 447 mA/mm (329 mA/mm) and a maximum transconductance of 525 mS/mm (145 mS/mm), respectively. Apparently, the device A shows better characteristics than the device B. In particular, a two-stage drain current and transconductance region appears in the device A, while only one-stage region is observed in the device B. The device mechanism and difference of the two devices will be described as follows.

Fig. 4, *a* and *b* reveal the corresponding energy-band diagrams from the middle of gate to buffer layer at equilibrium and $V_{GS} = +1\,V$ for the devices A and B, respectively. In the two devices, the depletion region of camel-like gate just immerses into the *n*-GaAs channel layer at equilibrium. Therefore, the two devices act as depletion-mode transistors. As a positive gate voltage is applied, the n^+-GaAs/p^+-GaAs junction is reverse bias, while the p^+-GaAs/*n*-GaAs junction is forward bias, as illustrated in the dashed lines. In the gate positive bias condition, the n^+-GaAs/p^+-GaAs junction absorbs somewhat gate voltage and a neutral region below gate appears. Though the n^+-GaAs cap layer is heavily doped, the metal-semiconductor junction still exists as the gate metal is deposited on the n^+-GaAs cap layer. That is to say, at gate positive bias the depletion region of metal-semiconductor junction will become smaller and somewhat neutral region with high electron concentration is formed within the 200 Å n^+-GaAs cap layer, even though the n^+-GaAs/p^+-GaAs junction is reverse bias.

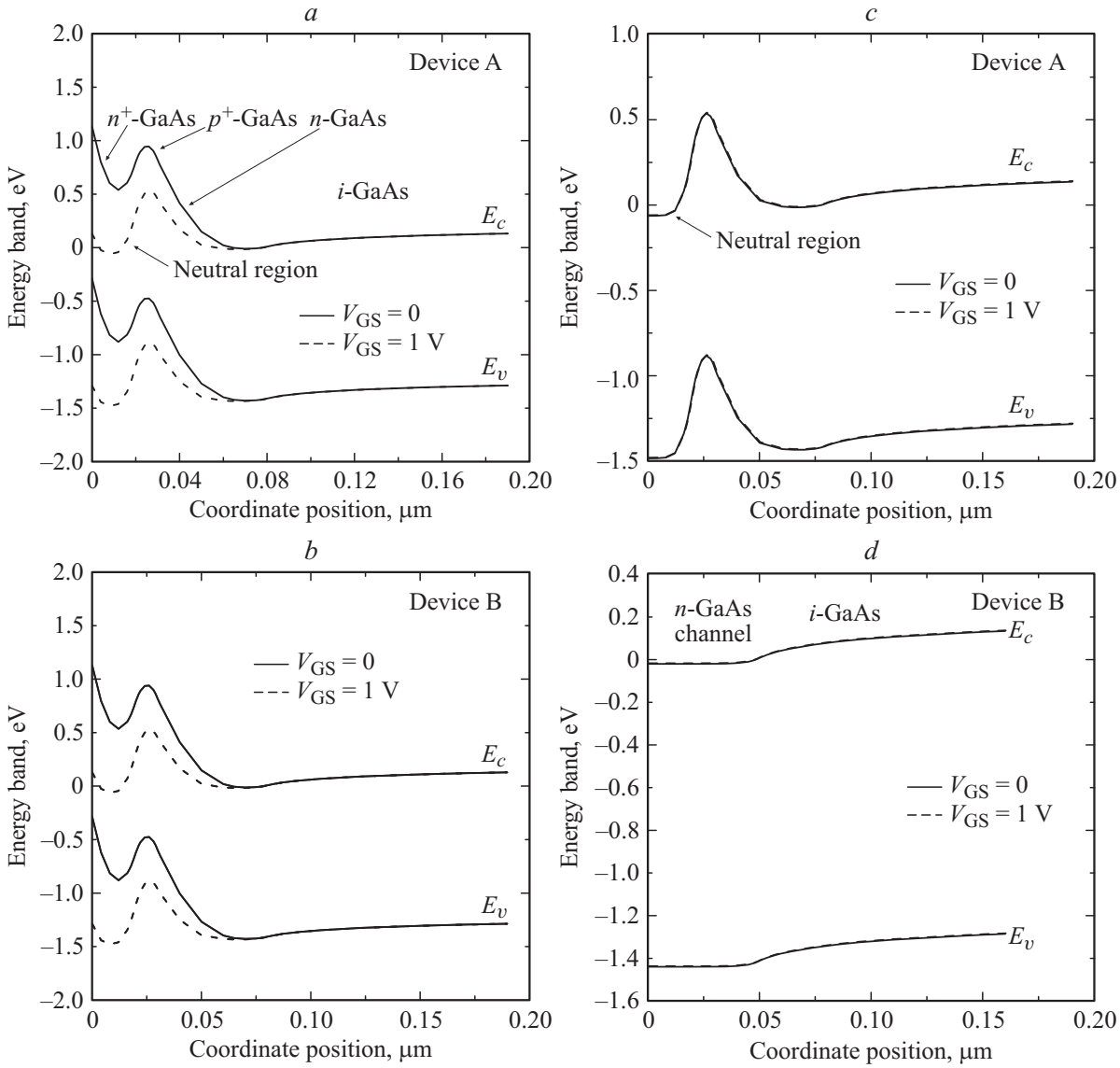

Figure 4. Corresponding energy-band diagrams at $V_{GS} = 0$ and $+1$ V. *a* — device A from the middle of gate to buffer layer; *b* — device B from the middle of gate to buffer layer; *c* — device A from the middle of gate-to-source region to buffer layer; *d* — device B from the middle of gate-to-source region to buffer layer.

On the other hand, the corresponding energy-band diagram from the middle of gate-to-source region to buffer layer at equilibrium and $V_{GS} = +1$ V for the devices A and B are depicted in Fig. 4, *c* and *d*, respectively. Clearly, a neutral region about 100 Å appears on the surface of the n^+-GaAs cap layer in the device A. Therefore, a second channel will be formed from source to drain electrodes through the n^+-GaAs cap layer at the positive bias. In other words, at large gate positive bias there are two conduction paths, i. e., the n-GaAs channel and n^+-GaAs cap layer, formed and a two-stage relationship between transconductance (current) versus gate voltage is observed in the device A, as illustrated in Fig. 3. While, only one conduction path, i. e., n-GaAs channel, exists at small gate bias, Nevertheless, in the device B there is only one-stage relationship because the n^+-GaAs cap layer at gate-to-source and gate-to-drain region has been removed. In addition, in the device A the extra carrier transportation route within the n^+-GaAs cap layer enable the drain current and transconductance to rapidly increase at $V_{GS} > +0.7$ V. Due to the higher channel concentration redulting from the extra carriers below the gate metal in device A, obvious gate leakage current is found at large gate-to-source positive bias. Also, as considering the application on signal linear amplification, the device B exhibits better relationship of voltage-independent transconductance than the device A though the maximum transconductance is lower.

4. CONCLUSION

The performance of GaAs homojunction camel-like gate FET with and without G-S and G-D recesses has been

successfully demonstrated and compared. The results show that device without G-S and G-D recesses exhibits larger output saturation current and higher transconductance for the formation of a second channel in the n^+-GaAs cap layer at large gate forward bias. On the other hand, the device with the recesses structure exhibits better relationship of voltage-independent transconductance. Consequently, the comparative study of the studied devices provides a promise for device design and circuit applications.

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