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Direct exchange between silicon nanocrystals and tunnel oxide traps under illumination on single electron photodetector

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In this paper we present the trapping of photogenerated charge carriers for 300 s resulted by their direct exchange under illumination between a few silicon nanocrystals (*ncs*-Si) embedded in an oxide tunnel layer ($\mathrm{SiO}_{x=1.5}$) and the tunnel oxide traps levels for a single electron photodetector (photo-SET or nanopixel). At first place, the presence of a photocurrent limited in the inversion zone under illumination in the I-V curves confirms the creation of a pair electron/hole (e-h) at high energy. This photogenerated charge carriers can be trapped in the oxide. Using the capacitance-voltage under illumination (the photo-CV measurements) we show a hysteresis chargement limited in the inversion area, indicating that the photo-generated charge carriers are stored at traps levels at the interface and within *ncs*-Si. The direct exchange of the photogenerated charge carriers between the interface traps levels and the *ncs*-Si contributed on the photo-memory effect for 300 s for our nanopixel at room temperature.

1. Introduction

The silicon (Si) is a low emitter of light because of its indirect bandgap. However, Si quantum dots may be good emitters of light. Indeed, Canham and colleagues [1,2] reported the photoluminescence of porous silicon (Si) in 1990, thus giving rise to a significant interest in the possibility of using Si, as light emitting material, as the base of computer chips. As Si requires high temperatures to crystallize, colloidal synthesis techniques have remained a challenge. High-quality Si nanocrystals (*ncs*-Si) have been synthesized by aerosol routes [3,4] as well as by etching of annealed silicon-rich oxides [5,6]. Alkyl-passivated colloidal *ncs*-Si has been reported with visible wavelength photoluminescence quantum yields of up to 60% [3]. LEDs made with *ncs*-Si (with ITO:PEDOT:TPD:Si ncs:Alq3:LiF/Al structure) achieved EQE of 8.6% — the highest of any ncLED to date [7]. However, spectral dependence of these devices on device current was noticed and attributed to the nanocrystal's polydispersity. Si nanocrystal-based LEDs with nearly identical structure to the device used for this study had only 0.8% EQE, but the photoluminescent quantum yield of the nanocrystals used in those devices was only 3% [8].

Because of the challenges with synthesis that Si nanocrystals have faced, the development of LEDs using these materials is much less mature than that of ncLEDs of CdSe nanocrystals. Therefore, it is not yet clear what the limitations of the technology will be in terms of brightness, color tunability, and efficiency. Insipte of that, advancement in this direction is likely to occur thanks to the significant recent advances in Silicon synthesis [5] in addition to potential advantages that Si has over CdSe including its abundance in nature and its non-toxicity. The single electron devices such as the single electron transistors have several suggested applications, both in the analog and digital domain. Some of them definitely attract more interest for their applicability in the consumer electronics such as the single-electron memory which is an interesting application [9]. Indeed, the use of a single electron transistor (SET), whose structure is similar to current CMOS memory cells, as a memory will allow for very low power consumption, and high integration due to its reduced size. Using a single electron device allows measurements based on the charge of a single electron, meaning that an ultra sensitive device could be achieved. Another application includes very narrow band SET oscillators which could be used for radio frequency systems. For digital applications there have also been suggestions for voltage state and charge state logic circuitry [10]. The detection of reduced number of photons is another SET application [11–13]. In order to increase the sensitivity of single photon detection, a new type of device is the objective of research and development:

the photo detector based on single electron transistor; photo-SET [14–16]. The development of usable photon counters is aimed at exploring new directions of research. Interaction with photons for SETs is an important subject for future applications such as quantum computing, medical imaging and other novel optoelectronic devices. Under light illumination, the absorbed photons can change the number of electrons in the dots, thus sensibly modulating the current level [17]. The telegraph noise may lead to decoherence and loss of readout's fidelity. This noise, which originates from the switching of charge between metastable trapping sites, remarkably increases when device sizes approach nanoscale [18,19]. Therefore, it is needed to understand the origin of noise and the mechanisms behind it. The study of RTS, which provided a powerful means of investigating the capture and kinetics emission of single defects and demonstrated the possible origins, is generally believed to be the weighted sum of many independent noise sources that physically correspond to fluctuating charge traps or defects. RTS signal in small area transistors has been a favourite tool in the study of individual traps in the silicon-silicon dioxide system [20–22]. The capacitance-voltage characterization (C-V) is another technique of characterization which has been extensively studied. Recently a new method for this characterization has been adapted: the photo-CV [23]. It is a technique requiring the same C-V procedure as any regular C-V technique but the device under test is subject to illumination. This technique can be used for the determination of interface properties [24–26] and also in silicon devices [27]. The photo-CV method has been among the characteristics used with Gwang et al. [28] for study the evolution with time of interface trap density and bulk density of states in amorphous-indium-gallium- zinc-oxide thin-film transistors (TFTs), for negative- bias-under-illumination-stress. In 2014 Chen et al. demonstrated the enhancement of the photo sensitivity of Si-based metal-oxide-semiconductor (MOS) tunneling photodiode with an ultra-thin SiO_2 layer [29].

Using a C-V and I-V measurements, we confirm the creation of photogenerated charge carriers under illumination, and their contribution in the photo-memory effect on the single electron photodetector. The analysis of photogenerated random telegraph signal is detailed in [30]. This study confirms the exchange possible of photogenerated charge carriers between the ncs-Si and the interface traps levels. This exchange leads to a photo-memory for a 300 s in the photo detector based on single electron transistor.

2. Experimental details

The single electron photo detector (Photo-SET) or nanopixel was developed in the Sherbrook University combining nanolithography and reactive ion etching (RIE) process. The schematic cross-sectional structure of nanopixel device discussed in this paper is shown in Fig. 1, *a*. We report the fabrication and insulation of nanopillars in which a layer of silicon rich oxide (SRO) deposited by low-pressure chemical-vapor deposition (LPCVD) is present between two layers of highly doped polysilicon. The nanocrystals are formed by annealing the SRO in nitrogen environment. After the annealing, Si dots appear in thick and thin layers. The oxide is composed of silicon nanocrystals (Si-ncs) embedded in $SO_{x=1.5}$ layer. The thick $SiO_{x=1.5}$ layer, where the ncs-Si density is about $1.6 \cdot 10^{11}\,cm^2$, presents spherical Si crystallites with an average size around 5 nm extracted from transmission electron microscopy (TEM) measurements. A second annealing step in oxygen was also performed. We used e-beam lithography and dry etching to obtain the vertical structures. These nanopillars are fabricated with diameters of $2\,\mu$m, 500 nm, 200 nm and 100 nm. The Fig. 1, *b* shows the scanning electron microscopy (SEM) image of nanopillar with 500 nm diameter. It is possible to get structures as small as 50 nm in diameter thus containing about 2–4 nc-Si. The electrical insulation is provided by planar photosensitive resist: it was spun and then etched back by O_2 plasma. Then chromium/gold electrodes were deposited by lift-off on the top of the columns. The substrate is used for electrical continuity.

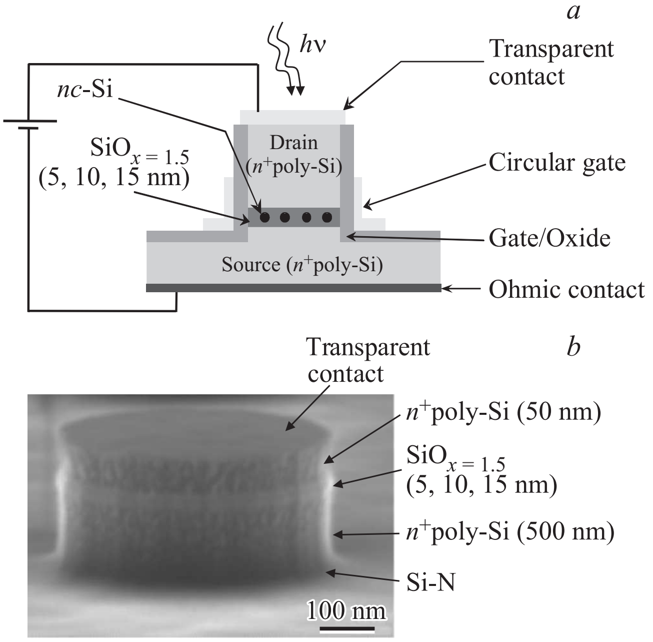

Figure 1. *a* — the schematic cross-sectional structure of nanopixel (Photo-SET); *b* — SEM micrograph of nanopixel with 100 nm diameter.

3. Results and discussions

3.1. I-V measurements

The current-voltage (I-V) measurements were registered using a Keithley 238, in the darkness and under illumination for different wavelength between 400 and 600 nm, while

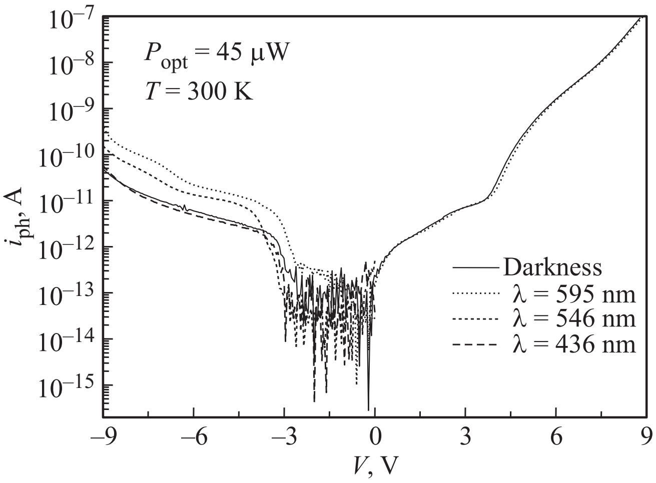

Figure 2. The current-voltage (I-V) measurements of nanopixel registered in the darkness and under illumination for different wavelengths.

sweeping the electrical polarization between (–9 V, 9 V) (Fig. 2). We note a limited photocurrent in the inversion area. Otherwise, the photocurrent increases when increasing the wavelength. When photogenerated charge carriers are created, they can pass into the oxide and may also be trapped. At a low or medium electric field, the *ncs*-Si can serve relay of conduction via the oxide layer. We consider now photons having an energy larger than silicon's bandgap. When reaching the space charge region, these photons are absorbed by the silicon nanocrystals and $(e-h)$ pairs are created. These pairs $(e-h)$ may spend in the oxide or be trapped. In the inversion zone, the existence of electric field may generate the separation of pairs $(e-h)$ and the photocurrent limited in this zone may be due to direct exchange of the photogenrated charge carriers between photogenerated traps [30] and the *ncs*-Si. These phenomena contribute to the detection process of a nanopixel [31].

3.2. Photo-CV measurements

ITO contacts have been formed by lift-off; they have served as mask for RIE etching of poly-Si, $SO_{x=1.5}$ and Si substrate. The photo-CV measurements have been performed using HP 4280A C Meter/1 MHz C-V Plotter by going alternately from inversion to accumulation and vice versa in the darkness and under illumination.

Fig. 3 shows the Capacitance-Voltage (C-V) characteristics at room temperature in darkness and under illumination where we can distinguish three areas: inversion, depletion and accumulation zones that are well described in [32]. In this study, we show an offset towards negative voltages under illumination that indicates the presence of positive charge (holes in our case) in the oxide tunnel layer and at the SiO_2/Si interface.

The photo-CV measurements (C-V measurements after light excitation) were carried out at different wavelengths between 400 and 600 nm at room temperature and for optical power equal to 100 μW (Fig. 4). We note the presence of a hysteresis only in the inversion zone which may be due to the storage of photogenerated carriers in the *ncs*-Si and/or the interface traps levels during their displacement.

The hysteresis loading is proportional to the incident number photons of given by [33]:

$$N_{\text{photon}} = (\lambda/hc)(1-R)[1-\exp(-\alpha t_{\text{dot}})],$$

were h — Planck's constant, c — speed of light in vacuum, R — Fresnel reflectance of the silicon surface, α — absorption coefficient of the silicon layer and t_{dot} — height of the silicon island.

Generally, the holes' trapping in the oxide tunnel layer is at the origin of the displacement of the photo-CV curves to negative voltages and chargement of a hysteresis. Such trapping is caused by a change in the internal structure of

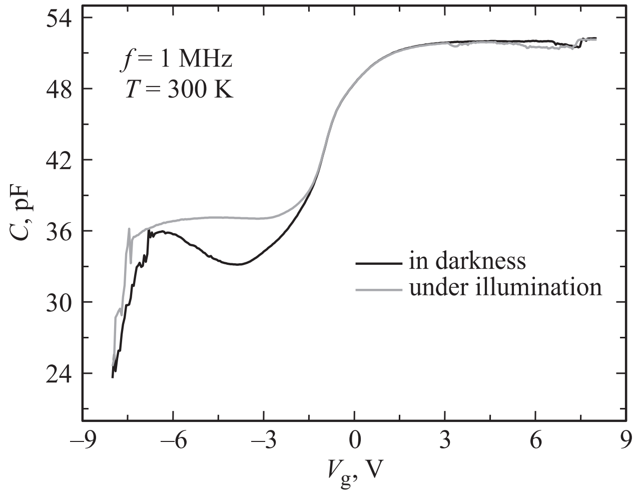

Figure 3. The C-V characteristic of a nanopixel in darkness and under illumination at room temperature.

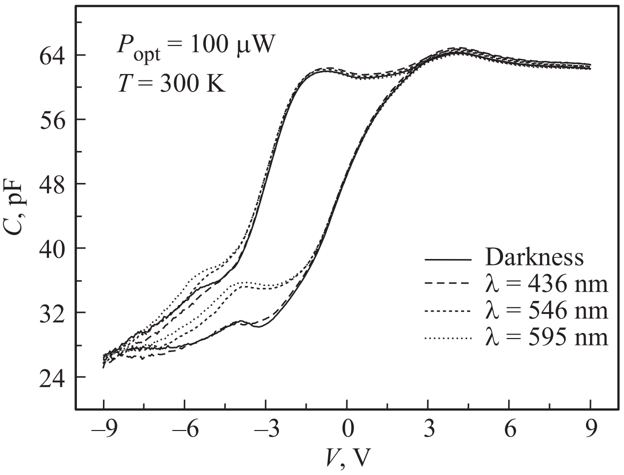

Figure 4. The photo-CV characteristics for a nanopixel at room temperature.

the oxide and the appearance of interface states under the effect of stress. The interface states' chargement depends on the charge exchange beteween the valence and conduction band of silicon. In other words, it depends on the position of the Fermi level at the interface [29] and consequently on the conditions of preparation of the oxide.

In our case this charging may be due to the exchange of photogenerated charge carriers between the *ncs*-Si and the interface traps in the oxide tunnel layer. In order to find the storage time [34] of photogenerated charge carriers in the *nsc*-Si, we visualize the variation effect of the voltage sweep rate on the photo-CV characteristic (Fig. 5). We notice an almost stable hysteresis chargement with increasing the time of light excitation on our devices. So the *ncs*-Si photocharging with a charge carrier's photogenerated via the oxide traps (exchange possible between them) will be made of an almost stable manner. For a ramp speed less than 20*m* V/s, this charging reaches saturation.

In Fig. 6, we visualized the charge trapping kinetics variation as function of time (flat-band variation as function of time). The storage time of photogenerated charge carriers on the *ncs*-Si is distorted by their exchange time with the oxide traps. This exchange occurs a time about a 300 s at room temperature. So a photo-memory effect (photogenerated charge carriers storage in the *ncs*-Si via the trap oxide) for the single electron photodetector based on single electron transistor (photo-SET) is highlighted.

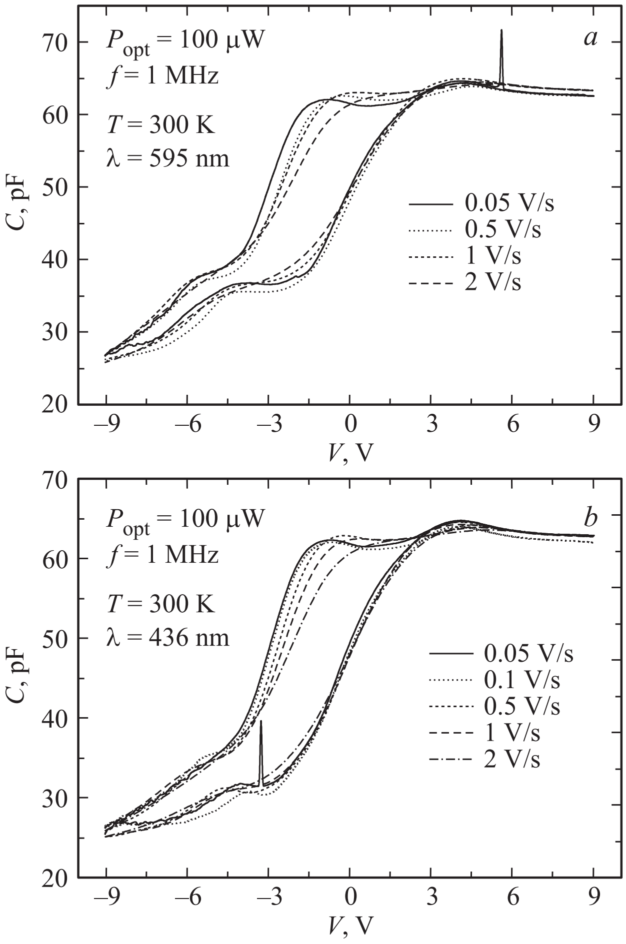

Figure 5. The effect of ramp speed variation on the photo-CV characteristics nanopixel at room temperature (*a*) for 595 nm (*b*) and for 436 nm.

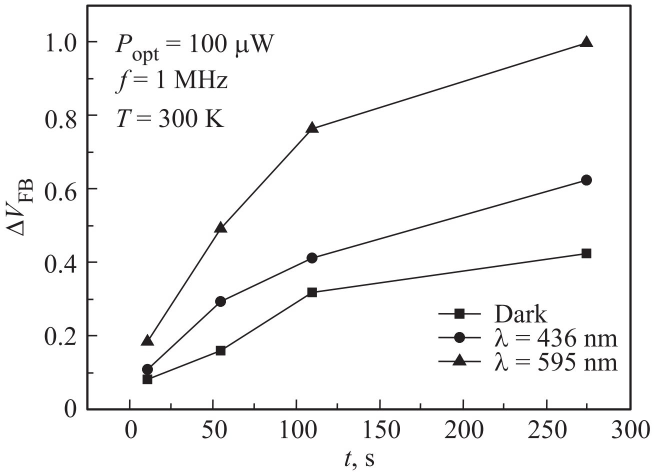

Figure 6. The flat band time variation (charge trapping kinetics).

4. Conclusion

Sensitive electrical measurements of I-V and C-V were used to investigate the exchange of photogenerated charge carriers in a single electron photodetector with a few *nc*-Si dots. Experiments showed that contribution of *nc*-Si was dominant for the capture of the photogenerated charge carriers. These traps contribute to determine the phototrapping process. This process is due to the dominance of tunneling of electrons from traps levels to the *nc*-Si. For our device the photo-trapping time is estimated to be about 300 s at room temperature. This phototrapping could be an attractive way for photo-memory application.

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