

Single electron transistor: energy-level broadening effect and thermionic contribution

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In this paper, a theoretical study of single electron transistor (SET) based on silicon quantum dot (Si-QD) has been studied. We have used a novel approach based on the orthodox theory. We studied the energy-level broadening effect on the performance of the SET, where the tunnel resistance depends on the discrete energy. We have investigated the I–V curves, taking into account the effects of the energy-level broadening, temperature and bias voltage. The presence of Coulomb blockade phenomena and its role to obtain the negative differential resistance (NDR) have been also outlined.

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1. Introduction

Recently, The integration of nano-devices in circuits or systems dealing with advanced functions, has been developed to perform processing and information transport technology. Among the new device concepts proposed for nanoscale architectures, the single electron transistor is a very promising one [1–3]. It has been made to overcome the problem of power consumption and to open the way for building nanoscale architectures. Different materials have been used to realize SET devices such as metals [4], semiconductors [5], carbon nanotubes, [6], graphene [7] and single molecules [8,9]. Furthermore, SET device has been performed to obey many required applications such as logic device [10], radio–frequency [11], gas sensor [12] and single electron memory [13]. The investigated device operates on the principle of Coulomb blockade [14], which is more prominent at nanoscale. The electronic characteristic of SET is totally different from classical one due to the presence of tunnel junctions. The gate electrode, capacitively coupled with the island, is used to control the charges transfer. As in the Coulomb blockade regime, the electron is carried by sequential tunneling from source to drain through the island. The average number of electrons on the island can change discretely due to quantum mechanical effects and electron–electron interaction. We notice that this concept has been reported in previous works by Miralaei et al. [15] and Mahapatra [16,17].

In this paper, we have studied the influence of different physical and electrical parameters on the I–V characteristic of SET simulated using a new approach. We have discovered an additive properties in the I–V characteristics of SET such as negative differential resistance (NDR) behavior. These electronic properties give us the possibility to realize nano-electronic devices in the future such as gate logic and single memory device.

This paper has been divided into two sections described as follows: in section 2, we have presented a new

mathematical model of SET based silicon quantum dot taking into consideration the tunnel current and thermionic contribution; in section 3, our simulation results have been discussed.

2. Model Description

A. Tunnel Current Calculation

In order to understand the phenomena occurred for the SET semiconductor, many models have been used. Based on the analytical approach given by M. Miralaei et al. [15], the tunnel resistance depends mainly on the discrete energy. The last condition gives birth to a novel orthodox theory approach. The tunneling rate from the source to the drain was calculated according to the orthodox theory and the tunnelling resistance. A lot of approximations are used [10–15] to improve our model. For that, we have considered a system with a double-junction. The free energy will be determined by:

$$\Delta F_{s,i} = \frac{e}{C_{\text{tot}}} \left(C_D V_{DS} + C_G V_{GS} - Ne - \frac{e}{2} - \lambda e \right) - \left(\frac{N+1}{2} \right) \Delta E,$$

$$\Delta F_{i,s} = \frac{e}{C_{\text{tot}}} \left(-C_D V_{DS} + C_G V_{GS} + Ne - \frac{e}{2} - \lambda e \right) - \left(\frac{N+1}{2} \right) \Delta E,$$

$$\Delta F_{i,d} = \frac{e}{C_{\text{tot}}} \left((C_G + C_{DS}) V_{DS} + C_G V_G + Ne - \frac{e}{2} - \lambda e \right) - \left(\frac{N+1}{2} \right) \Delta E,$$

$$\Delta F_{d,i} = \frac{e}{C_{\text{tot}}} \left(-(C_G + C_{DS})V_{DS} + C_G V_G - Ne - \frac{e}{2} - \lambda e \right) - \left(\frac{N+1}{2} \right) \Delta E, \quad (1)$$

where, N is a number given by

$$N \begin{cases} n+1 & \text{if } n \text{ even,} \\ n, & \text{if } n \text{ odd,} \end{cases}$$

e is the electron charge, C_{tot} is the total island capacitance, λ is a real number that presents the background charge, n — the number of electrons in the island, C_G , C_D and C_S represent respectively, the gate, drain and source capacitance. We notice that the total island capacitance C_{dot} in the 2D structure per array becomes $(4C_{\text{tot}} + C_G)/2$. For the 3D structure it is equal to $(5C_{\text{tot}} + C_G)/3$ for the upper and over planes and $2C_{\text{tot}}$ for the planes between them due to the series and parallel combination of C_{tot} .

To adjust the first energy level to the Fermi level of the source-drain electrodes, we have calculated the energy, that equal to $\Delta E + E_c/2$ ($E_c = e^2/C_{\text{tot}}$). Where, ΔE is the energy required for the electron to move from the highest level occupied to the lowest unoccupied level of the island [18]. The tunneling rate can be written in a general form using the Helmholtz free energy ΔF and Fermi's golden rule [11,13–16]:

$$\Gamma(n, n+1) = \frac{2\pi}{h} \int_{-\infty}^{+\infty} \int_{-\infty}^{+\infty} |T|^2 D_i(E_i) D_f(E_f) f(E_f) \times (1 - f(E_f)) \delta(E_i - E_f - \Delta F) dE_f dE_i. \quad (2)$$

Where, h is the Planck constant, Γ is the total tunneling rate across the barrier from the side i of the occupied initial state in the metallic electrode to the side f of the unoccupied final state in the island. E_i , E_f , D_i and D_f are respectively the energies and densities of the initial and final state (DOS). In fact, $f(E_f)$ is the Fermi–Dirac distribution that gives the occupation probability of energy levels, $|T|^2$ represents the tunneling transmission coefficient. Therefore, $(1 - f(E_f))$ is the probability of finding an empty state. The equation can be simplified as follow [15]:

$$\Gamma(n, n+1) = \frac{2\pi}{h} t_{if}(E) \frac{-\Delta F}{(1 - \exp(\Delta F/K_B T))}. \quad (3)$$

Where, t_{if} is defined as the tunneling transmission probability between the initial and final state and it is composed of the product of D_i , D_f , and the tunneling transmission coefficient $|T|^2$. In case of metallic islands, the probability of tunneling transmission is considered as constant for all energy levels. In contrast, for molecules or semiconductor islands, the energy level broadening can be modeled through Lorentzian function taking into account the tunneling transmission probability as follows [11,13,14]

$$t_{i,f}(E) = \sum_n \alpha \frac{(\gamma_n/2)^2}{(E - E_n)^2 + (\gamma_n/2)^2}. \quad (4)$$

Where, $(n = 0, 1, 2, 3, \dots)$ are discrete energy levels (due to quantization) in the semiconductor island that can be

obtained by solving the Schrödinger equation. γ_n represents a parameter related to the „escape frequency“ of an electron from the island (a term used for any particular energy state to indicate the amount of broadening) that describes the half-width of the DOS peaks. The transmittance strength parameter allows us to classify tunnel barriers according to their transparency, i.e. width and height.

Neglecting charging effects, the tunnel junction has an Ohmic I–V characteristic. It can be defined by a phenomenological quantity, namely the „tunneling resistance“, $R_T = V/I$. The presence of a current through the junction is proportional to the bias voltage applied across the junction.

Therefore, from the tunneling transmission probability and discrete energy levels [15], the tunneling discrete resistance is given by Eq. (5):

$$R_t^{\text{discrete}} = \frac{h}{2\pi e^2 t_{i,f}(E)}. \quad (5)$$

Using the orthodox theory [18–23] and [19–23] equations described above (Eq. (3)–(5)), the expression for the transmission rate will be:

$$\Gamma(n, n+1) = \frac{-\Delta F}{e^2 R_t^{\text{discrete}} (1 - \exp(\Delta F/k_B T))}. \quad (6)$$

In this paper, we have taken into account the basic concept of the energy level broadening. Therefore, using the Eq. (6), the tunneling rate is modified for discrete energy levels as follows:

$$\Gamma_n^{\text{discrete}} = \Gamma^{\text{orthodox}} \left(\frac{\alpha \frac{(\gamma_n/2)^2}{(E - E_n)^2 + (\gamma_n/2)^2}}{t_{i,f}^{\text{orthodox}}} \right). \quad (7)$$

In order to test our model, we have used MATLAB simulator. The current's expression is calculated using the master equation described in details in Ref. [20–22].

B. Thermionic Contribution

At high-temperature operation, the electrons are thermally excited and move freely in a parallel channel through the SET. To get a better understanding of the relationship between the transport properties and the temperature contribution, we have considered the thermionic emission effect [14] which is described below:

$$I_{D\text{thermionic}}(V) = S J_{\text{thermionic}}$$

$$= AS \frac{m_{\text{ox}}}{m_0} T^2 \left[\frac{-e \left(\varphi_0 - \sqrt{\frac{eV_{DS}}{4\pi\epsilon_0\epsilon_r}} \right)}{k_B T} \right]. \quad (8)$$

Where, k_B is the Boltzmann constant, E is the electric field and ϵ_r is the relative dielectric permittivity.

The structural parameters of our simulated device are summarized in Table.

Electronic parameters description of the SET

Description	Value
A constant effective Richardson S Junction area	$1.20173 \cdot 10^6 \text{ A} \cdot \text{m}^{-2} \cdot \text{K}^{-2}$
m_{ox} mass of the electron in the oxide TiO_x	$10 \cdot 2 \text{ nm}$
ϵ_0 vacuum permittivity	$0.40m_0$
ϵ_r relative permittivity of the dielectric TiO_x	$8.854 \ 187 \ 817 \cdot 10^{-12} \text{ F/m}$
ϕ_0 barrier height Ti/TiO_x	3.5
Dielectric thickness	0.35 eV
SET drain capacitance, C_D	8 nm
SET source capacitance, C_S	0.062 aF
SET gate capacitance, C_G	0.062 aF
	0.24 aF

We notice that $C_{\text{tot}} = 0.362 \text{ aF}$, the charging energy $E_C = e^2/2C_{\text{tot}} \approx 0.432 \text{ eV} > 10k_B T$ for $T = 300 \text{ K}$. The final current through the SET can be defined as the sum of the tunnel and the thermionic currents:

$$I_{\text{TOT}}(V) = I_{\text{tunnel current}} + I_{\text{thermionic}}. \quad (9)$$

The three-dimensional (3D) structure of the simulated SET device is shown in Fig 1.

The developed analytical model of the I – V characteristics of Single Electron Transistor is described in section 3.

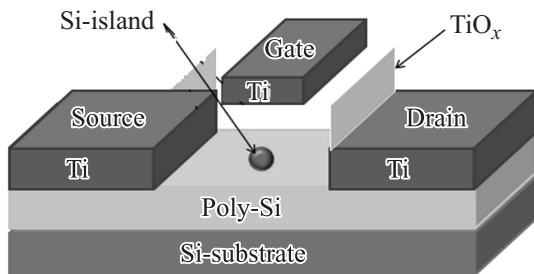


Figure 1. 3D-Structure of Single Electron transistor.

3. Results and discussion

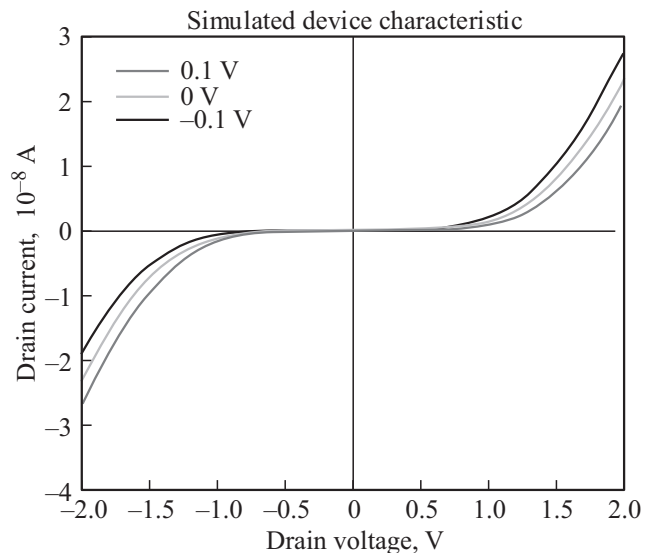
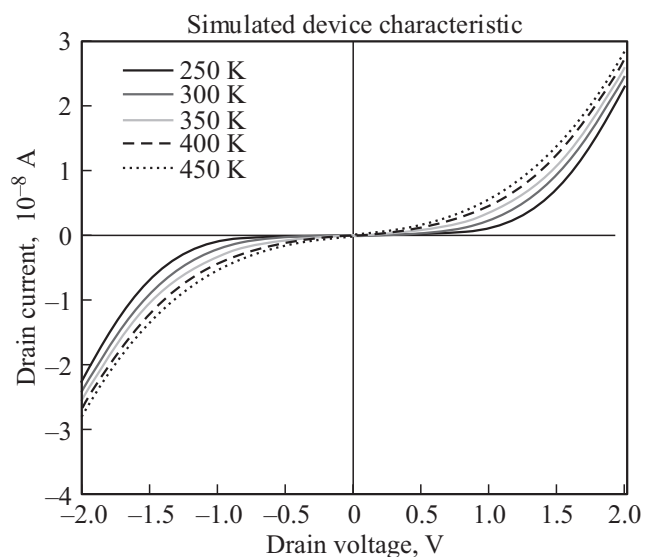
In this section, the result of simulating a SET has been investigated. We have taken into account that the tunnel junction resistance depends on the discrete energy, which leads to a novel orthodox theory approach. When a bias voltage is equal to zero, the Fermi levels of both electrodes are in the equilibrium state which lead to the absence of current flow. This absence of the electron tunneling at low bias condition is called coulomb blockade. Once external voltage V_{DS} is applied above the threshold voltage, the tunneling of an electron between the source to drain via the quantum dot was obtained.

The simulation results illustrated in Fig. 2 reveal a strong field effect in the conductance of the gate voltage. The

modulated current is established by changing the polarity of gate field that leads to a variation of the QD Fermi level. As a consequence, the current flows between source and drain, it can be controlled by the gate voltage.

Generally, at high temperature, thermally activated electron transport occurs by thermionic emission. The I – V_{DS} characteristic shows that changing the temperature has a remarkable effect on the electrical characteristics and especially in the Coulomb blockade area. Fig. 3 depicts the I – V_{DS} characteristics for different temperatures. At high temperature, we can see there are no coulomb blockade effect which is generally explained by the thermionic contribution.

Fig. 4 and 5 shows the I – V_G characteristics for different temperatures and source–drain voltage, respectively. The I – V characteristics has a periodic function namely

Figure 2. I – V_{DS} characteristic of gate voltage effect on source–drain currents.Figure 3. I – V_{DS} characteristics for different temperature.

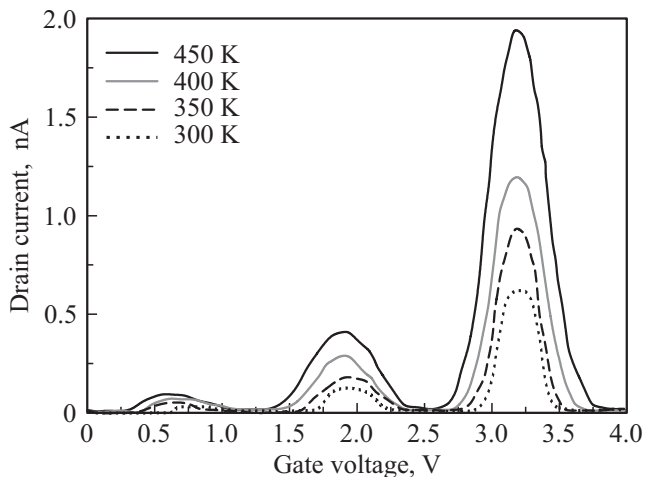


Figure 4. $I-V_{GS}$ characteristics for different temperatures.

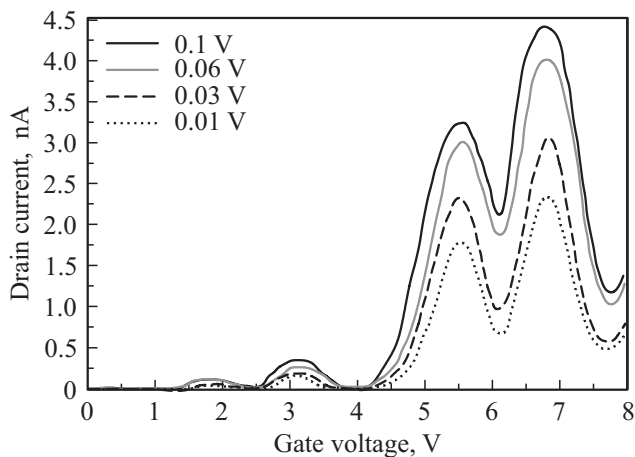


Figure 5. $I-V_G$ characteristics of source-drain voltage effect on source-drain currents.

Coulomb blockade oscillation. One can easily distinguish the effect of variation of energy level broadening. As we know, in the metallic QD, a single energy level lead to equality of the current peaks [24,26]. However, in semiconductor QD, the current peaks are not equal, due to the contribution of broadening of energy level.

The rise of gate voltage leads to increase of the current value peaks. This can be explained by the increasing of the number of electrons in the QD and the role of broadening of energy level. At high temperature, the electron transport is thermally activated. As result, the current increases due to the thermionic contribution.

The simulation of $I-V_G$ characteristics at 300 K for different source-drain voltages is illustrated in Fig 5. When V_{DS} voltage increases up to threshold voltage electron tunnels from source to drain via dot. The increasing of drain voltages plays a crucial role to increase the electron tunnel. As a result, The current is enhanced.

Additionally, the negative differential resistance (NDR) effect has been investigated. It defines as a negative slope

region of the $I-V$ curve. An increase in voltage across the device's terminals results in a decrease in current through it.

The coulomb oscillation curves and NDR behavior are well shown in Fig. 5. They depend on the Coulomb interaction between electrons and the effect of the discrete resistance (R_i^{discrete}). The NDR effect is observed on the $I-V_G$ curve. It can be explained by the tunnelling through discrete quantum-mechanical state and a small density of state (DOS) of the quantum dot levels. The electron tunnelling from the dot decreases from one electrode to the other one. These give us a non-linear current resulting in the NDR effect.

4. Conclusions

To sum up, the single electron transistor has been simulated using MATLAB simulator. A novel orthodox theory approach in which a non equal energy level broadening was considered. Different tunneling current rates for distinct energy levels of the Silicon QD have been demonstrated. Using this model, we have found that the total current is the sum of the tunneling and the thermionic currents. The investigation of the $I-V$ curves leads to conclusion that the energy level broadening affects the Coulomb oscillation by changing the current peak value. Our device can be operated at high temperature required for many applications in the field of nano-electronics with stability and low power dissipation in the future. We note that the negative differential resistance effects could be highly useful in the miniaturization of a wide variety of applications such as in memory cells, analog-to-digital converter, RF oscillators, logic circuit and cellular neural network.

References

- [1] I.I. Abramov, E.G. Novik. Semiconductors, **35** (4), 474 (2001).
- [2] I.I. Abramov, E.G. Novik. Semiconductors, **33** (11), 1254 (1999).
- [3] I.I. Abramov, E.G. Novik. Semiconductors, **34** (8), 975 (2000).
- [4] K.G. El Hajjam, M.A. Bounouar, N. Baboux, S. Ecoffey, M. Guilmain, E. Puyoo, L.A. Francis, A. Souifi, D. Drouin, F. Calmon. IEEE Trans. Electron Dev., **62** (9), 2998 (2015).
- [5] S. Chatbouri, M. Troudi, N. Sghaier, A. Kalboussi, V. Aimez, D. Drouin, A. Souifi. Semiconductors, **50** (9), 1163 (2016).
- [6] H.W.C. Postma. Science, **293** (5527), 76 (2001).
- [7] J.A. Mol, C.S. Lau, W.J.M. Lewis, H. Sadeghi, C. Roche, A. Cnossen, J.H. Warner, C.J. Lambert, H.L. Anderson, G.A.D. Briggs. Nanoscale, **7** (31), 13181 (2015).
- [8] M.L. Perrin, E. Burzurí, H.S.J. van der Zant. Chem. Soc. Rev., **44** (4), 902 (2015).
- [9] T.T. Phuc. J. Phys. Conf. Ser., **187**, 12055 (2009).
- [10] K. Maeda, N. Okabayashi, S. Kano, S. Takeshita, D. Tanaka, M. Sakamoto, T. Teranishi, Y. Majima. ACS Nano, **6** (3), 2798 (2012).
- [11] R.J. Schoelkopf. Science, **280** (5367), 1238 (1998).
- [12] P.S.K. Karre, M. Acharya, W.R. Knudsen, P.L. Bergstrom. IEEE Sens. J., **8** (6), 797 (20080).

- [13] „compact-modeling-of-single-electron-memory-based-on-perceptron-designs-2169-0022-1000187.pdf.crdownload“.
- [14] N.T. Bagraev, E.I. Chaikina, E.Y. Danilovskii, D.S. Gets, L.E. Klyachkin, T.V. L'vova, A.M. Malyarenko. *Semiconductors*, **50** (4), 466 (2016).
- [15] M. Miralaic, M. Leilaoui, K. Abbasian, *J. Electron. Mater.*, **42** (1), 47 (2013).
- [16] S. Mahapatra, V. Vaish, C. Wasshuber, K. Banerjee, A.M. Ionescu. *IEEE Trans. Electron Dev.*, **51** (11), 1772 (2004).
- [17] S.S. Dan, S. Mahapatra. *IEEE Trans. Electron Dev.*, **56** (8), 1562 (2009).
- [18] S.S. Dan, S. Mahapatra. *IEEE Trans. Nanotechnol.*, **9** (1), 38 (2010).
- [19] H. Grabert, M.H. Devoret. (Eds) *Single Charge Tunneling* (Boston, MA, Springer US, 1992) v. 294.
- [20] C. Wasshuber. *Computational Single-Electronics* (Viennam, Springer Vienna, 2001).
- [21] S. Datta. *Electronic Transport in Mesoscopic Systems* (Cambridge, Cambridge University Press, 1995).
- [22] S. Kano, K. Maeda, D. Tanaka, M. Sakamoto, T. Teranishi, Y. Majima. *J. Appl. Phys.*, **118** (13), 134304 (2015).
- [23] M. Chakraverty, R. Chakravarty, V. Babu, K. Gupta. *Adv. Sci. Eng. Med.*, **8** (7), 552 (2016).
- [24] K.G. El Hajjam, M.A. Bounouar, N. Baboux, S. Ecoffey, M. Guilmain, E. Puyoo, L.A. Francis, A. Souifi, D. Drouin, F. Calmon. *IEEE Trans. Electron Dev.*, **62** (9), 2998 (2015).
- [25] X. Wang, W. Porod. *VLSI Des.*, **13** (1–4), 189 (2001).
- [26] A. Boubaker, M. Troudi, N. Sghaier, A. Souifi, N. Baboux, A. Kalboussi. *Microelectronics J.*, **40** (3), 543 (2009).

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