Thermally deposited Ag-doped CdS transistors with rare-earth oxide Nd_2O_3 as gate dielectric

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The performance of thermally deposited CdS thin film transistors doped with Ag has been reported. Ag-doped CdS thin films have been prepared using chemical method. High dielectric constant rare earth oxide Nd_2O_3 has been used as gate insulator. The thin film trasistors are fabricated in coplanar electrode structure on ultrasonically cleaned glass substrates with a channel length of 50 μm. The thin film transistors exhibit a high mobility of 4.3 $cm^2V^{-1}s^{-1}$ and low threshold voltage of 1 V. The ON-OFF ratio of the thin film transistors is found as 10^5. The transistors also exhibit good transconductance and gain band-width product of $1.15 \cdot 10^{-3}$ mho and 71 kHz respectively.

1. Introduction

In the recent years, thin film transistors (TFTs) are widely used as switching devices in large area electronics circuits. In active matrix liquid crystal displays (AMLCDs) technology, TFTs are used to control each pixel individually. The TFTs can be regarded as th driver in the liquid crystal displays. The driving capability of the devices is directly proportional to the field-effect mobility of the TFTs. High field-effect mobility of the carrier in the channel region increase the switching speed of the transistors and low threshold voltage reduce the power consumptions of the TFTs. To achieve high frame rate in high resolution displays, enhanced drain current of the TFTs is required. Increased drain current is the result of high field-effect mobility and low threshold voltage. Hence the threshold voltage needs to be lowered and the field-effect mobility of the carrier in the channel needs to be increased.

Up till now, many attempts have been made by the investigators to improve the carrier mobility of the TFTs. Though amorphous silicon is widely used in liquid crystal displays, but it could not provide adequate performance and reliability is some current controlled devices [1]. Therefore search for alternative semiconductor as active material with high filed-effect mobility in the channel of TFTs is still going on.

CdS have become one of the most promising semiconductor materials that could be used as active material in TFTs. Evaporated CdS thin films have been used by many investigators with varying digress of success in the early development of TFTs [2–5]. High mobility *n*-channel TFTs have been reported with spin coated CdS thin films [6]. Recently, interests have been grown to fabricate chemically deposited CdS thin films to use as TFT's channel material that provide a low temperature and large-area compatible processing technique. TFTs with chemically deposited CdS active layer have been reported successfully [1,7,8].

The performance of TFTs depends on semiconductor–insulator combinations. Thermally deposited silicon dioxide is the most promising dielectric material in TFTs, but the operating voltage of silicon dioxide insulated TFTs is large. For portable applications, especially for radio frequency identification, devices required low power consumptions and hence the operating voltage needs to be lowered below 5 V [9]. The reduction of threshold voltage is the key to lower the operating voltage of the devices. One of the main technical trends to lowering the operating voltage is the use of high dielectric constant (k) gate dielectric.

It has been reported that the rare earth oxides Nd_2O_3, Er_2O_3, Pr_2O_3, ZrO_2, La_2O_3 etc. exhibited very high dielectric constant and low leakage current and hence reliable for gate dielectric in microelectronics [10,11]. Among the different rare-earth oxides Nd_2O_3 has been under intence investigation as gate dielectric recently for replasing for conventional SiO_2 due to its high dielectric constant and low leakage current. In this investigation we chose the thermal evaporation technique for fabrication of the TFTs. This is due to the fact that, among the different techniques such as chemical vapour deposition, atomic layer deposition, sol-gel techniques, electron beam deposition etc. that used to deposit thin films, thermal evaporation is a well-known and rather gentle technique that does not produce any kind of surface damage [12,13]. Kannan et al. [14,15] reported that the thermally deposited Nd_2O_3 thin films show well amorphous structure. Moreover amorphous dielectric films are usually insensitive to impurities [16] and more stable owing to the absence of grain foundaries hence suitable for gate insulator.

Further in this investigation in order to improve the field-effect mobility of the TFTs Ag-doped CdS thin films have been used as active material. It has been reported that the resistivity of CdS thin films can be abruptly reduced by doping of Ag into it [17]. Here the output responses of the *p*-type Ag-doped CdS TFTs with Nd_2O_3 as gate dielectric has been reported.

2. Experimental

2.1. Preparation of Ag-doped thin films

For the preparation of Ag-doped CdS thin films, CdS and $AgNO_3$ of analytical grade purity are used without

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further purification. CdS thin films of thickness 550 Å are deposited on glass substrates using thermal evaporation technique. $AgNO_3$ solutions of five different concentrations (1mmol/L−5mmol/L) are prepared by dissolving $AgNO_3$ powder in double distilled water and the mixture is stirred at room temperature using magnetic stirrer. The deposited CdS thin films are treated chemically by immerginin in $AgNO_3$ solution of five different concentrations separately for 60 s. The doping of Ag in the CdS films is confirmed by change is colour of the films from orange-yellow due to the diffusion of Ag in to CdS. Doping of Ag in CdS thin films occurred by ion exchange process in which Cd^+ cations in CdS thin films are exchanged by Ag^+ cations from $AgNO_3$ solution when CdS thin films are immerged into it [18]. The films after immersion are cleaned in distilled water and died. The $AgNO_3$-treated CdS films are then annealed in vacuum at 400°C for 1 h.

2.2. Fabrication of the thin film transistors

The TFTs are fabricated in coplanar electrode structure on perfectly cleaned glass substrates using thermal evaporation technique under high vacuum. A 50 μm channel length is prodeced using a wire grill fixed on the mask. The general fabrication procedure of the TFTs involves the following steps:

i) Al is deposited over the Ga-doped CdS thin films as source-drain electrodes.

ii) Over source−drain electrodes Nd_2O_3 of thickness 900 Å is deposited as gate dielectric layer.

iii) Over the dielectric layer, again Al is deposited as gate electrode.

The schematic diagram of coplanar electrode structure of the fabricated devices is shown in Fig. 1. The thicknesses of the films are measured by Tolansky method [19] (multiple beam interference method).

3. Characterization of the CdS thin films

The presence of Ag in the CdS thin films is confirmed from the XRD results shown in Fig. 2. A distinct peak of Ag_2S (103) is observed in the X-ray diffraction (XRD) pattern which confirms the presence of Ag in CdS films. A large diffraction peak of (002) and the smaller peaks (101), (102) and (103) correspond to the hexagonal structure of CdS are also observed in the XRD pattern. Fig. 3 shows the EDS of the Ag-doped CdS thin film which also confirms the presence of Ag in the CdS.

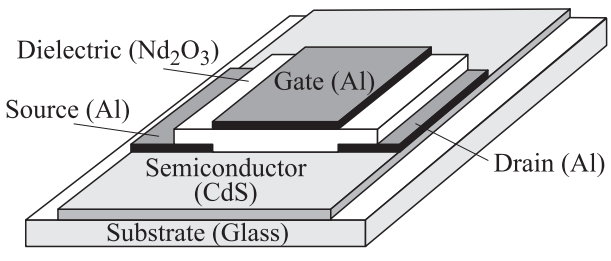

Figure 1. Schematic structure of the coplanar electrode structure of the thin film transistor.

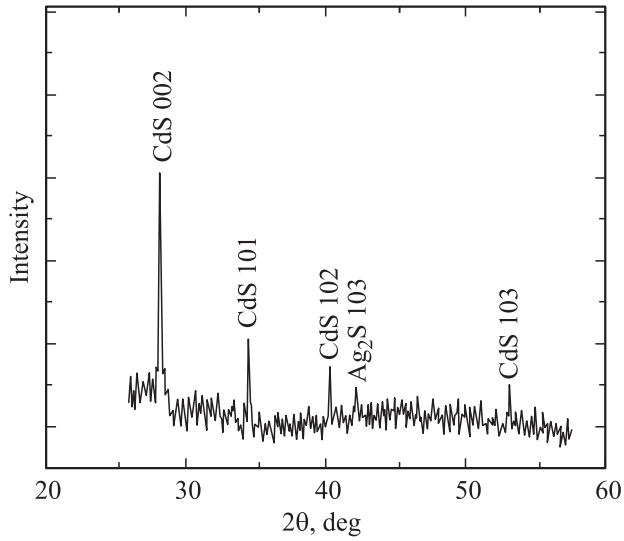

Figure 2. X-ray diffraction spectrum of the Ag-doped CdS thin film.

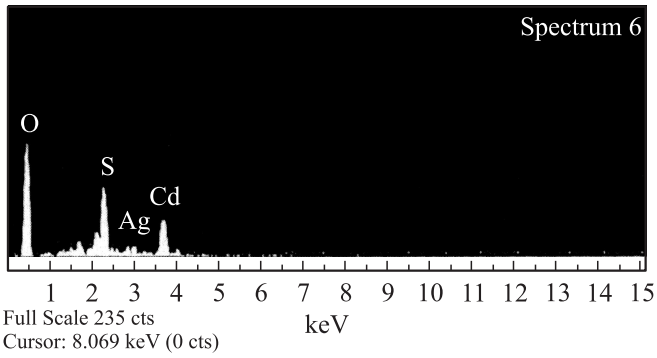

Figure 3. EDS spectra of Ag-doped CdS thin film.

4. Results and discussions

Well-modulated I_D-V_D characteristics of the TFTs at various gate voltages (V_G) is shown in Fig. 4. TFTs prepared using the CdS films immerged into $AgNO_3$ solutions of 5 mmol/L concentrations for 60 s show the maximum drain current and also better electrical properties. Hence performance of the TFTs with CdS thin films treated with $AgNO_3$ solutions of 5 mmol/L concentration is presented in this paper.

Fig. 5 represents the $(I_d)^{1/2}-V_G$ plots for Ag-doped TFTs at constant drain voltage $V_D = 6$ V. From the extrapolation of the linear portion of graph to the V_G axis of plot, the threshold voltage (V_T) of the devices is calculated. In saturation region $V_D-V_G-V_T$, the drain current is given

Measured values of mobility (μ_{FET}), threshold voltage (V_T) transconductance (g_m), gain-bandwidth product ($G \cdot Bw$) and ON-OFF ratio of the fabricated devices and comparison of some results with the previous work.

Device type	Mobility, μ_{FET} ($cm^2V^{-1}S^{-1}$)	Threshold voltage (V_T)	Transconductance, g_m (mho) ($V_D = 6$ V)	Gain-bandwidth product, $G \cdot Bw$ (kHz)	ON-OFF ratio
Undoped CdS-TFT (previous work)	$1.6 \cdot 10^{-2}$	–	$5 \cdot 10^{-5}$	6.74	–
Ag-doped CdS-FTT (present work)	4.3	1	$1.15 \cdot 10^{-3}$	71	10^5

by equation [20]

$$I_{D\,sat} = \frac{W}{2L}\mu_{FET}C_i(V_G - V_T)^2 \qquad (1)$$

where W is the channel width, L is channel length, C_i is the gate capacitance per unit area, V_T is the threshold voltage and μ_{FET} is the field-effect mobility. The field-effect mobility μ_{FET} is calculated from the slope of this plot.

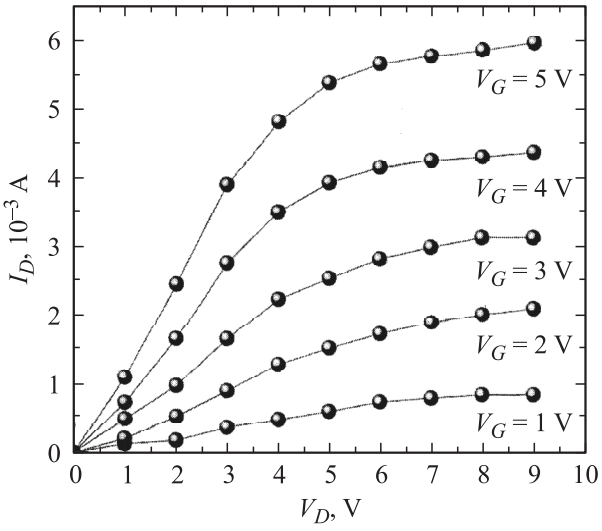

Figure 4. $I_D - V_D$ characteristics of Ag-doped CdS TFTs at constant V_G.

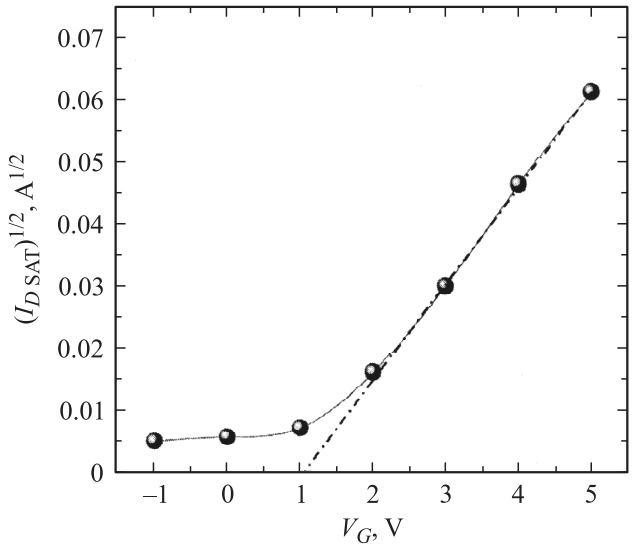

Figure 5. $\sqrt{I_d} - V_G$ plots for Ag-doped TFTs as constant drain voltage $V_D = 6$ V.

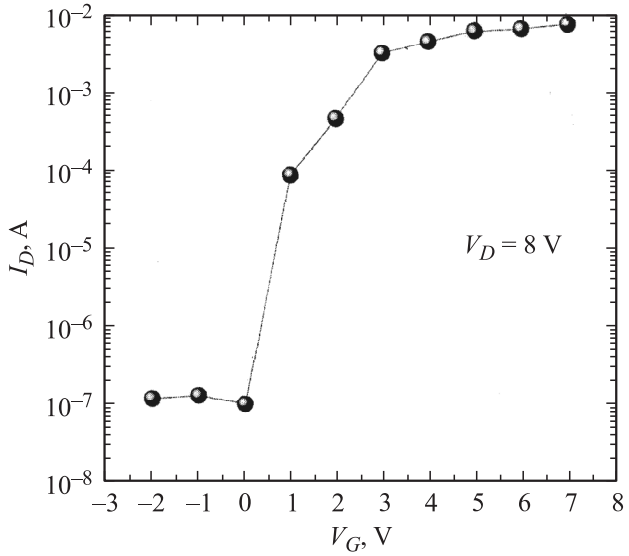

Figure 6. The plot of $I_D - V_G$ at constant drain voltage (8 V).

The transconductance (g_m) which is a measure of current carrying capability of the TFTs is given by equation [20]:

$$g_m = \left(\frac{\partial I_D}{\partial V_G}\right)_{V_D=\text{const}} = \frac{WC_i}{L}\mu_{FET}V_D. \qquad (2)$$

The gain-bandwidth ($G \cdot Bw$) product of the devices is evaluated equation [21]:

$$GBw = \frac{g_m}{2\pi C_i}. \qquad (3)$$

The plot of I_D at a constant drain voltage (8 V) is shown in the Fig. 6. The ON-OFF ratio of the device is calculated from the relation [20]:

$$\frac{I_{ON}}{I_{OFF}} = \frac{C_i\mu_{FET}(V_G - V_T)^2}{\sigma d V_D}, \qquad (4)$$

where σ and d are conductivity and thichness of the semiconductor of the TFTs.

The calculated values of mobility, threshold voltage, transconductance, gain band-width product and ON-OFF ratio of the devies are presented in table. Table also

shows a comparison of some of the results of the present investigation with the results of undoped CdS–Nd_2O_3 TFTs reported by previous workers [4].

The high field effect mobility of the devices is due to the doping of Ag in CdS thin films which decrease the resistivity of the films. Initially the Ag atoms are on the surface of the films. As the films are annealed to 400°C, the Ag atoms diffused inside of thin films [17]. Due to diffusion of Ag atoms the grain boundary states in the case of the polycrystalline CdS (poly-CdS) films are passivated by Ag atoms which complete some of the open bonds (dangling bonds) at grain boundaries. Consequently the interface states density drops and the potential barrier is lowered. The resulting effect is that the poly-CdS electrically progresses towards single crystal CdS characteristics, yielding higher mobility.

The threshold voltage of the TFTs is also found low. The Ag-doped TFT exhibits a high gain-bandwidth product which is the measure of high frequency perfomance of the devices. The high gain bandwidth product of the devices is due to hight field-effect mobility.

5. Conclusions

Frin the comparison of the result of the present investigation with the results of the previous worker present in table, it is observed that the Ag-doped CdS TFTs established their superiority than that of the undoped CdS TFTs. A set of high drain current is observed in case of Ag-doped TFTs which is due to high mobility and low threshold voltage It may also be concluded that the fabrication of Ag-doped CdS TFTs with high -dielectric constant Nd_2O_3 as gate dielectric is certainly feasible.

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