Effect of Submicron Structural Parameters on the Performance of a Multi-Diode CMOS Compatible Silicon Avalanche Photodetector

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We present a theoretical study on gain and bandwidth of a CMOS-compatible submicron multi-diode Si avalanche photo-detector suitable for operation at high speed and moderate voltage. A two-dimensional model is used to obtain the avalanche build-up of carriers in the depleted region considering the dead-space effect. The regions between fingers are discretized to sub-regions, and the carriers are specified by their energy and position indices. The model also considers the effects of carriers diffusion from the substrate region, and the parasitic effects due to the presence of multiple diodes in lateral configuration. The gain and frequency response data obtained from the model are shown to be in good agreement with experimental data taken from literature. The results are shown for variation of gain and bandwidth with substrate thickness, finger spacing, and number of diodes. It has also been shown that there exists optimum choice of substrate thickness so that the gain?bandwidth product reaches maximum keeping other parameters constant.

Keywords: dead-space effect, impact ionization, lateral CMOS $p-i-n$, Si-avalanche photo-detector, gain-bandwidth.

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