Silicon Nanowire Parameter Extraction Using DFT and Comparative Performance Analysis of SiNWFET and CNTFET Devices

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The performance and scalability of silicon nanowire field-effect transistor (SiNWFET) and carbon nanotube field-effect transistor (CNTFET) with surround gate geometry are studied using such tools as material exploration and design analysis (MedeA) and device modeling and simulation SilvacoTCAD. The SiNWFET and CNTFET with gate-all-around (GAA) structure offer good gate electrostatic control, high On-current, and better suppression of short-channel effects with complete encirclement of the device channel. Rather than using the bulk properties of silicon, estimation of properties SiNW was made using MedeA VASP tool based on density functional theory (DFT). In this study, the device input (I_D-V_{GS}) and output (I_D-V_{DS}) have been analyzed and parameters like threshold voltage, I_{On}/I_{Off} ratio, drain induced barrier lowering, and sub-threshold slope extracted, and comparison is made between SiNWFET and CNTFET devices. The results point towards the DFT-based material parameter estimation to incorporate the quantum effects and usage of SiNW/CNT-based GAA structure utility below 10 nm to meet scaling targets. The results suggest that the SiNWFET and CNTFET device with GAA geometry could be better alternative to conventional MOSFETs and FinFET for numerous high-performance and low-power device applications.

Keywords: SiNWFET, CNTFET, FINFET, DFT, VASP, TCAD.

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