Performance Evaluation of Inversion Mode and Junctionless Dual-Material Double-Surrounding Gate Si Nanotube MOSFET for 5-nm Gate Length

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In this work, drain current I_D for 5-nm gate length with dual-material (DM) double-surrounding gate (DSG) inversion mode (IM) and junctionless (JL) silicon nanotube (SiNT) MOSFET have been studied and simulation results are reported using Silvaco ATLAS 3D TCAD. For this work, we used the non-equilibrium Green's function (NEGF) approach and self-consistent solution of Poisson's equation with Schrödinger's equation. The conduction band splitting into multiple sub-bands has been considered and there is no doping in channel in case of IM SiNT MOSFET. The effect of DM gate engineering for SiNT channel radius 1.5 nm with 0.8-nm gate oxide (SiO_2) thickness on I_D has been studied. A comparison of results has been done between IM DM DSG and JL DM DSG CGAA SiNT. In case of JL, doping concentration is optimized for two concerns: (i) to get the same I_{On} current as IM device and (ii) to get the same threshold voltage V_{Th} as IM. This has resulted in 10^2 and 10^3 times smaller I_{Off} in matching I_{On} and V_{Th} optimized device, respectively, as compared to IM. It is found that DM gate engineering reduces drain-induced barrier lowering (DIBL) for both IM and JL SiNT MOSFET. In this work, JL have much smaller DIBL $\sim$ 15 mV/V, almost an ideal SS $\sim$ 60 mV/dec, and higher I_{On}/I_{Off} ratio $\sim 2.18 \cdot 10^8$ as compared to available CGAA literature results.

Keywords: inversion mode, junctionless, DM DSG, Si nanotube MOSFET, NEGF, I_D, SS, DIBL.

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