Bulk Fin-FET Strategy at Distinct Nanometer Regime for Measurement of Short-Channel Effects

© S.M. Jagtap[1], V.J. Gond[2]

[1] E and TC Department, MVPS's KBT College of Engineering,
Nashik, India
[2] E and TC Department, MET's Trust Bhujbal Knowledge City College of Engineering,
Nashik, India

E-mail: sarikamg@gmail.com

Received October 5, 2020
Revised October 5, 2020
Accepted for publication October 29, 2020

The planar structure of MOSFET invites uncertainties that can't reduce the short-channel effects (SCE) like drain-induced barrier lowering (DIBL), punch through, and sub-threshold slope (SS). Fin-FET technology can be a better choice. It is a technology that uses more than one gate, called multiple gate devices, which is an improved technology option for further shrinking the size of the planar MOSFET. In this work, we inspect possibilities of gate-length and fin-thickness scaling in triple-gate single Fin-FET device design to solve the problem of short-channel effects and progress the performance of the nanoscale device. The electrical characteristic parameters of the nanoscale device like threshold voltage, subthreshold slope, drain-induced barrier lowering, and leakage current are evaluated from DC characteristics (transfer and output) by proposed design. The findings offer the drain-induced barrier lowering, threshold voltage, and leakage current by calculation. From the simulation results, we observe lowering of drain-induced barrier lowering, sub-threshold slope, and leakage current, whereas threshold voltages rise. A triple-gate N Fin-FET is designed with different fin thickness and gate length in scaling with 14, 10, and 7 nm, and the effects are observed on the improved performance of the device. 3D Single Fin-FET structure is designed successfully, and we plot the current–voltage $I(V)$ characteristics and transfer characteristics.

Keywords: SCE, modeling, BSIM-CMG, ITRS, DIBL, threshold voltage.

Full text of the paper will appear in journal SEMICONDUCTORS.