The analysis of leakage current in MIS Au/SiO_2/*n*-GaAs at room temperature

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The aim of this study is to determine the reverse-bias leakage current conduction mechanisms in Au/SiO_2/*n*-GaAs metal–insulator–semiconductor type Schottky contacts. Reverse-bias current-voltage measurements ($I-V$) were performed at room temperature. The using of leakage current values in SiO_2 at electric fields of 1.46–3.53 MV/cm, $\ln(J/E)$ vs. $\sqrt{E}$ graph showed good linearity. From this plot, dielectric constant of SiO_2 was calculated as 3.7 and this value is perfect agreement with 3.9 which is value of SiO_2 dielectric constant. This indicates, Poole–Frenkel type emission mechanism is dominant in this field region. On the other hand, electric fields between 0.06–0.73 and 0.79–1.45 MV/cm, dominant leakage current mechanisms were found as ohmic type conduction and space charge limited conduction, respectively.

1. Introduction

Silicon dioxide (SiO_2) as a gate dielectric has played an important role in development of fundamental devices for microelectronics and semiconductor industries. Also SiO_2 dielectric material will continue to be an important part of new-generation gate stacks as an intermediate layer between silicon and high permittivity (high-k) dielectrics [1]. But for high frequency and low power applications, semiconductor materials of devices must have higher saturated electron velocity and higher electron mobility. Because of GaAs has these electrical properties, much attention has been focused on the fabrication of GaAs based oxide devices with various insulator layers such as SiO_2 that is deposited with plasma enhanced chemical vapor deposition (PECVD) [2–5].

In addition, the reverse-bias leakage current is an important parameter for device applications that degrades the electrical performance. It is necessary to demonstrate what conduction mechanisms are dominant in the device to reduce leakage current.

In this study we focused on the sources of reverse-bias leakage current in Au/SiO_2/*n*-GaAs metal–insulator–semiconductor (MIS) type Schottky contacts (SCs) with SiO_2 thicknesses of 30 Å at the room temperature. By the analysis of the leakage current-voltage ($I-V$) characteristics of SCs, different leakage current conduction mechanisms were found in different oxide field ranges were presented.

2. Experimental Method

Au/SiO_2/*n*-GaAs SCs were fabricated on quarter of the 5.08 cm diameter float zone (100) *n*-type GaAs wafer having thickness of about 350 μm with $(2-3)\cdot 10^{18}$ cm^{-3} carrier concentrations. For the fabrication process, the firstly GaAs wafers were dipped in ammonium peroxide for a few seconds to remove native oxide layer on the surface. Au/Ge/Ni alloy was evaporated onto the whole back side of the wafer at a pressure about 10^{-7} Torr in a vacuum system. In order to perform the ohmic contact, wafer was sintered at 430°C for 40 s. Insulator layer (SiO_2) was coated on the upper surface of the GaAs by using plasma enhanced chemical vapor deposition (PECVD) technique. The wafer was placed in the vacuum system after SiO_2 coated and high purity gold (Au) front (Scottky contacts) with a thickness of 1500 Å were evaporated at a rate of on the $\sim$ 2 Å/s through a metal shadow masks with circular dots of 1 mm diameter. The metal layer thickness and the deposition rates were monitored with the help of quartz crystal thickness monitor. After the SiO_2 coating, the surface characterization was carried out with atomic force microscopy (AFM).

The current-voltage ($I-V$) characteristics of the Au/SiO_2/*n*-GaAs SCs were measured at room temperature using a Keithley 220 programmable constant current source and Keithley 614 electrometer in dark conditions. All measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card. The $C-V$ measurements were performed by using an HP 4192A LF impedance analyzer at 5 kHz and 1 MHz and small sinusoidal test signal of 40 mV from the external pulse generator was applied to the samples in order to meet the requirement.

3. Results and discussion

AFM is a useful technique for characterizing the surface properties of the thin films. After SiO_2 coating, the surface morphology and roughness of SiO_2 were measured using the AFM technique. Imaging was performed in the vacuum chamber. Fig. 1 shows AFM image with a 4 μm^2 scan area recorded from the SiO_2 cap layer surface of the structure. From the measurement, root mean square (RMS) roughness was found as 0.12 nm = 1.2 Å. That means the surface of SiO_2 was atomically flat, namely perfectly smooth. As can

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be seen from Fig. 1, there is hardly visible porosity on the surface of SiO_2 because of the density of porosity is very low. The degree of porosity affects the dielectric constant of material [6]. As known, high porosity causes low dielectric constant due to the addition of new electrical paths. The physical aspects of SiO_2 surface are very well as it has low porosity degree. Although surface morphology of SiO_2 looks good, the examination of leakage current requires the formation of interfacial states, chemical defects, etc.

The leakage current of Au/SiO_2/*n*-GaAs SCs as a function of gate voltage at room temperature was given in Fig. 2. As can be seen from Fig. 2, leakage current increases with applied negative voltage. An ideal dielectric film having a thickness sufficiently large so as not to allow direct tunneling will show no appreciable leakage current [7]. But there are several sources of leakage current conduction mechansims. For example, because of SiO_2 dielectric layer may have defect states, some field enhanced thermionic

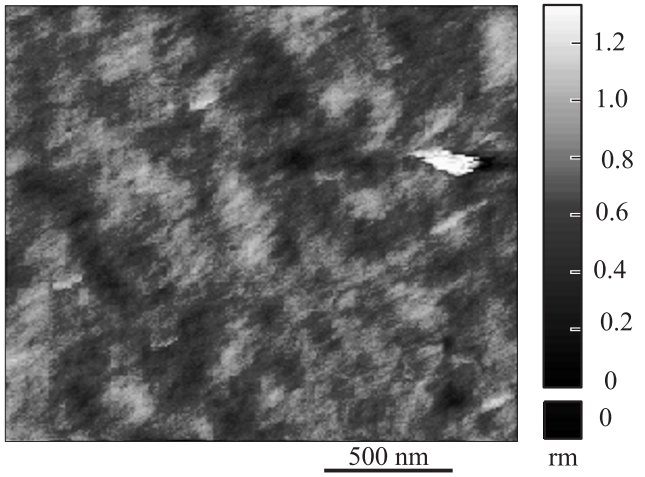

Figure 1. AFM image of SiO_2 surface.

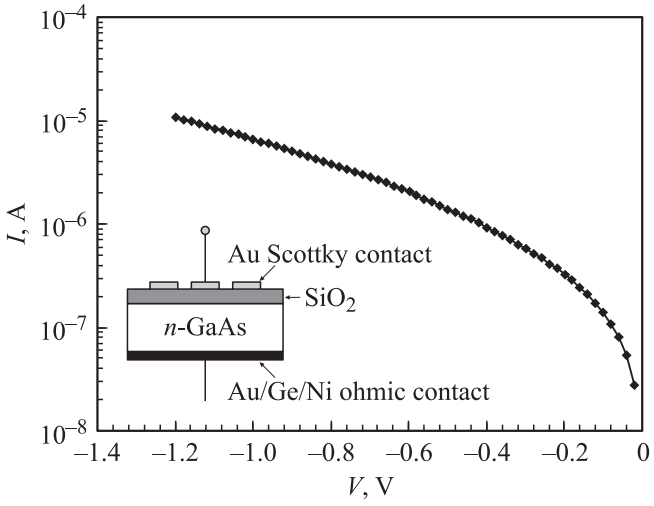

Figure 2. Reverse-bias semilogarithmic current–voltage characteristics of Au/SiO_2/*n*-GaAs SCs at 300 K (inset figure shows structure of the SCs).

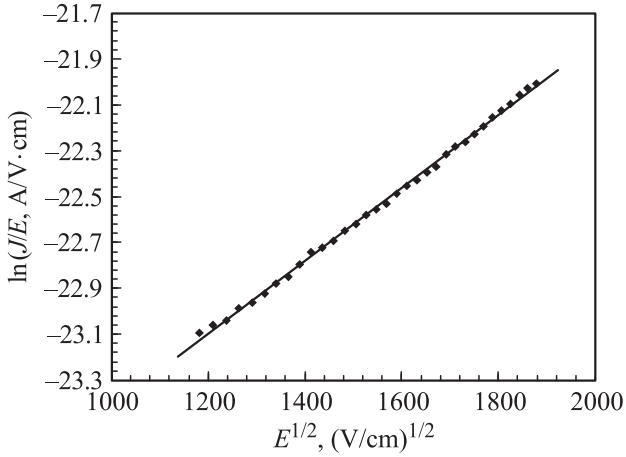

Figure 3. A plot of $\ln(J/E)$ vs. $\sqrt{E}$ at negative bias for Au/SiO_2/*n*-GaAs SCs.

emission of trapped electrons into the conduction band of dielectric called Poole–Frenkle emission dominates at fairly high electric fields [7]. The current due to Poole–Frenkle (PF) emission is given by

$$J_{\mathrm{PF}} = E \exp\left[-(q/kT)\left(\phi_t - \sqrt{qE/\pi\varepsilon_r\varepsilon_0}\right)\right], \qquad (1)$$

where J is the reverse bias current density, E is electric field, ϕ_t is the trap energy level below the conduction band edge of dielectric, and ε_r is the relative permittivity of the dielectric, T is the temperature, k is Boltzmann's constant, and ε_0 is the permittivity of free space. If the leakage current is governed by PF emission, a linear relation between $\ln(J/E)$ vs. $E^{1/2}$ with a slope of $\left(q\sqrt{qE/\pi\varepsilon_r\varepsilon_0}\right)/kT$ should be obtained [8].

Fig. 3 shows a plot of $\ln(J/E)$ vs. $E^{1/2}$ of the measured values, and as can be seen good linearity in the oxide field range of 1.46−3.53 MV/cm. From the slope of $\ln(J/E)$ vs. $E^{1/2}$, permittivity of the SiO_2 dielectric was found 3.7. This calculated value is perfect agreement with 3.9 which is permittivity of the SiO_2. Thus, reverse bias leakage current conduction between 1.46−3.53 MV/cm oxide field region can be described by Poole–Frenkle emission model.

From the intersection value of $\ln(J/E)$ vs. $E^{1/2}$ graph, the trap energy level $\phi_t = 0.64$ eV was obtained. As mentioned above, deposited dielectric layer may have a high density of structural defects. The structural defects cause additional energy states close to the band edge, called traps and current flow by these traps. Especially oxygen vacancies are known to be the dominant defect in deposited SiO_2 dielectric films [1,9]. As known, capacitance–coltage ($C-V$) characteristics are very sensitive to defects. Fig. 4 shows $C-V$ measurements of Au/SiO_2/*n*-GaAs SCs at low (5 kHz) and high (1 MHz) frequencies. As can be seen from Fig. 4, the diode capacitance decreases after reaching the peak. This anomalous $C-V$ characteristic is attributed to contribution of interface states or traps [10].

Fig. 5 shows $\ln(J)$ vs. $\ln(E)$ for Au/SiO_2/*n*-GaAs SCs at negative bias. The plots are linear at initially and low

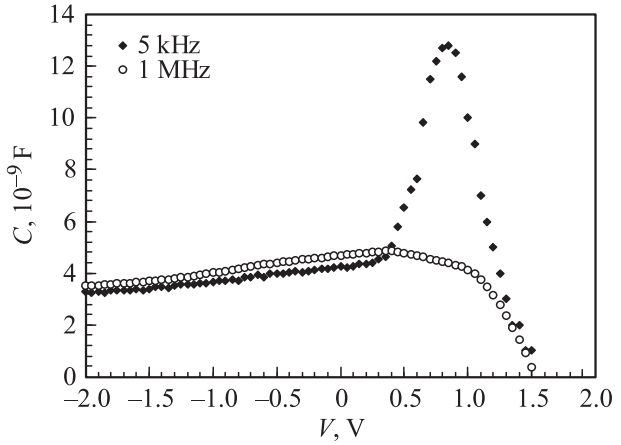

Figure 4. $C-V$ plots of low (5 kHz) and high (1 MHz) frequencies for Au/SiO_2/n-GaAs SCs.

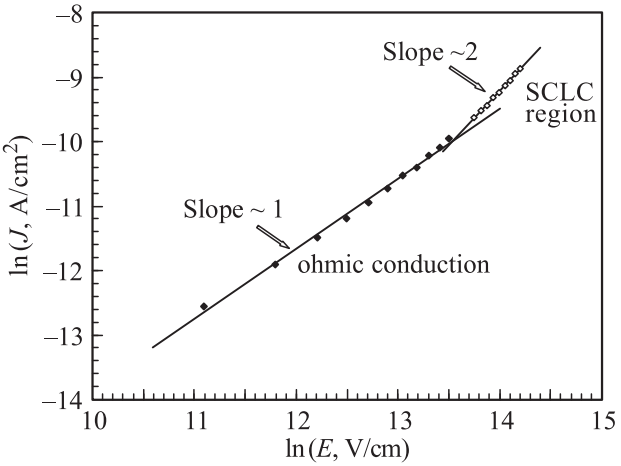

Figure 5. $\ln(J)$ vs. $\ln(E)$ plot at negative bias for Au/SiO_2/n-GaAs SCs.

electric field regions. At initially or lower bias region, the slope of the plot is around 1 that indicates ohmic conduction mechanism. Current conduction at initially electric field may be due to a hopping mechanism where leakage current related with thermally excited electrons [7].

Beyond this low electric field range the plot shows a second linear range but with a slope around 2, that indicates space charge limited conduction (SCLC) mechanism. As can be seen from Fig. 5, there is no any vertical regime whose slope is infinite that indicates the effect of discrete traps is surpassed by distributed traps. Thus, SCLC square law can be written as

$$J = \frac{9\mu\varepsilon_r\varepsilon_0 E^2}{8L}, \qquad (2)$$

where μ is charge mobility and L is the film thickness. From Eq. (2) mobility of the charges is calculated too small to transport all of charge carriers the remnant injected charge carrier will form a space charge to limit the current flow. Therefore, at the low electric field region charge carrier mobility is small and leakage current arises from SCLC mechanism [11].

4. Conclusion

To summarize, the analysis of leakage current conduction mechanisms of Au/SiO_2/n-GaAs SCs were discussed in this study. There are found that different conduction mechanisms are dominant in different oxide field range. Electric fields between 0.06−0.73 and 0.79−1.45 MV/cm, dominant leakage current mechanisms were found as ohmic type conduction and space charge limited conduction, respectively. At fairly high electric field region (1.46−3.53 MV/cm) Poole–Frenkel type emission mechanism was dominant. This process is related to emission of trapped electrons into the conduction band of SiO_2 dielectric.

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