Current Transfer in a Semiconductor Structure with a Porous Silicon Film formed by Metal-Stimulated Etching

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It is shown that during a porous Si film formation by metal-stimulated etching a barrier layer is formed on a monocrystal *p*-Si substrate. The rectifying properties of the semiconductor structure can be explained by the fixation of the Fermi level in the near-surface layer of porous Si due to a high concentration of electrically active defects (deep centers or traps). It causes to energy bands bending and the appearance of a potential barrier. The study of Raman scattering showed the absence of size effects and a change in the band gap in the porous Si film. Activation energies of deep centers by the temperature dependence of the current-voltage characteristics and deep level transient spectroscopy study were determined.

Keywords: porous silicon, deep level, Raman scattering, current-voltage characteristics, deep level transient spectroscopy.

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1. Introduction

At present, there is considerable interest in the field of studying the properties of porous silicon (*por*-Si) films for the purpose of their application in various fields of science and technology. One of the most important fields of application of *por*-Si films is the creation of antireflection coatings for silicon photoelectric solar energy converters [1]. For solar energy, the use of *por*-Si films fabricated by metal-stimulated etching is topical. This method provides the lowest reflectivity of the *por*-Si film surface compared to other methods (anodic electrochemical etching, chemical coloring etching), which contributes to an increase in solar cells efficiency [1–3]. The basis of the metal-stimulated etching method is the selective chemical etching of silicon using noble metal particles preliminarily deposited on its surface; silver and gold are most often used. Silicon etching proceeds directly under the metal particles in the solutions containing hydrofluoric acid and an oxidizing agent. As a result, a *por*-Si film is formed, which consists of filamentary silicon crystallites [4,5]. *Por*-Si films formed by metal-stimulated etching can be used to create the structures, which implement the surface-enhanced Raman scattering (SERS) effect, increase the sensitivity of molecular analysis [6,7]. In addition, such films can be used to create highly efficient thermal converters and anodes for lithium-ion batteries [6,8]. These areas of application of *por*-Si films grown by metal-stimulated etching are currently relevant. In connection with this circumstance, the problem of studying the physical processes occurring in semiconductor structures containing such films is topical. The main objective of this study is to develop a model of the current transport mechanisms in a semiconductor structure with a *por*-Si film fabricated by metal-stimulated etching, taking into account the microstructure of the porous film and the effect of traps with deep energy levels.

2. Samples and study methods

The *por*-Si film was grown by metal-stimulated etching using silver particles on a single-crystalline silicon wafer of *p*-conductivity type with a resistivity 1 Ohm · cm and surface orientation (100). During the first stage of the technological process, silver particles were deposited on the Si-wafer from the solution: Ag_2SO_4 (0.01 M), HF (46%), C_2H_5OH (92%) with mixture ratio 1 : 0.1 : 0.3. A drop of the solution was applied to one of the wafer surfaces and kept for 30 sec. At the second stage, a porous structure was formed. A wafer with pre-applied silver particles was immersed in a solution: H_2O_2 (1.24 M), HF (46%), C_2H_5OH (92%) with mixture ratio 1 : 0.5 : 0.25. The duration of etching was 20 min. After the first and second stages, the wafer was washed in distilled water in order to remove traces of technological solutions. At the final stage, the sample was washed for 15 min in concentrated nitric acid to remove silver particles from the porous film. To carry out electrical measurements, In ohmic

contacts were formed to the *por*-Si film and Si-substrate on opposite surfaces of the semiconductor structure.

In order to clarify the features of the microstructure of the *por*-Si film, the Raman scattering spectrum (RSS) method was used. The RSS spectra of the *por*-Si film and the single-crystalline substrate used to fabricate the experimental sample were measured near the first-order RSS of silicon ($520.6\,cm^{-1}$). RSS spectra were measured using a spectrometer U-1000 (Jobin Ivon). RSS excitation was done with Ar- laser emission at a wavelength of 488 nm, directed along the normal to the sample surface.

The features of current transfer mechanisms in a semiconductor structure were studied by measuring current-voltage characteristics (CVC) at various temperatures. For measurements, an experimental installation based on a closed-type helium cryostat Janis CCS 400/204N and electometer Keithley-6517B with a built-in controlled direct voltage source was used. The CVC were measured with forward and reverse bias in the temperature range $T = 70-370\,K$ with an increment of 10 K. A forward bias corresponds to the application of a negative potential to the contact on the surface of the *por*-Si layer, a positive potential — to the ohmic contact to *p*-Si on the opposite surface of the structure under study.

To study deep centers — traps of charge carriers with deep energy levels (DL), the method of current deep-level transient spectroscopy (I-DLTS) was used. We used a I-DLTS spectrometer specially adapted for studying samples of a relatively large area (electrical barrier capacitance) and high leakage currents [9], that is typical of the semiconductor structure under study.

3. Experiment and analysis of results

3.1. Results of Raman scattering spectra research

The RSS spectra of the surface of the *por*-Si film and silicon substrate are shown in Fig. 1. The position of the spectral maximum of the first-order RSS line of the substrate corresponds to the frequency of $520.6\,cm^{-1}$, which is typical of single-crystalline silicon. For the *por*-Si film, compared to the substrate, the first-order RSS line is shifted to the low-frequency region by $1.6\,cm^{-1}$, while the line shape remains symmetrical (Fig. 1). The width of the spectral line under consideration, determined at a level of 0.5 of the maximum intensity, for the *por*-Si film is by $0.6\,cm^{-1}$ greater, than for the substrate. The shift of the first-order RSS spectral line towards lower frequencies, accompanied by its expansion to the low-frequency region, is associated with the manifestation of the effect of spatial phonon confinement in silicon crystallites of the film *por*-Si [10–12]. In our case, the values of the shift of the first-order RSS spectral line to the low-frequency region and the broadening are small, therefore, the effect of the spatial limitation of phonons in the *por*-Si film does not manifest.

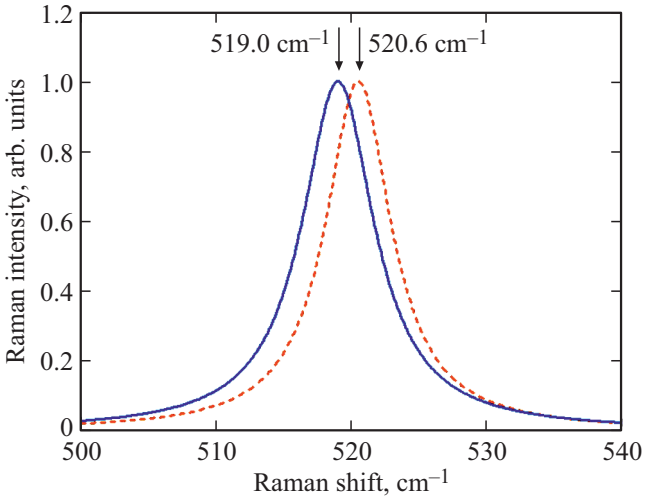

Figure 1. Raman scattering spectra of the *por*-Si film (solid line) and single-crystalline silicon substrate (dashed line) of the experimental sample.

The most probable reason explaining the observed behavior of the RSS spectra (Fig. 1) is the occurrence of tensile mechanical stresses as a result of the formation of *por*-Si film of the investigated semiconductor structure [13]. The growth of the *por*-Si film leads to the expansion of the silicon crystal lattice in the direction perpendicular to the sample surface [11,12]. The lattice deformation is mainly due to the misorientation of the planes perpendicular to the wafer surface [12]. In the study [11] the occurrence of deformations is explained by the high ratio of silicon crystallites surface area *por*-Si film to their volume.

The mechanical stress σ in the *por*-Si film can be estimated using the formula

$$\sigma = -52.7\Delta\omega, \qquad (1)$$

where $\Delta\omega = \omega - \omega_0$, ω_0 and ω — positions of the maxima of the first-order RSS spectral line of silicon in the absence and presence of mechanical stresses, consequently, the value σ is expressed in MPa [13]. For the sample under study $\omega = 519.0\,cm^{-1}$, $\omega_0 = 520.6\,cm^{-1}$, the value σ was 84.3 MPa.

3.2. The results of current-voltage characteristics study

The current-voltage characteristics of the semiconductor structure under study at different temperatures for forward and reverse bias are presented in Figs 2 and 3, respectively, as current density J dependences of the applied bias direct voltage U. For forward bias, the CVC branches are presented on a double logarithmic scale (Fig. 2), for reverse bias — on a linear scale (Fig. 3). It follows from Figs 2 and 3 that CVCs of the investigated semiconductor structure has a rectifying character. The value of the rectification coefficient, defined as the ratio of current densities at $U = 1.0\,V$ for

forward and reverse bias, decreases from 915.7 to 14.8 within the temperature range 70−370 K. At $T = 300$ K the rectification factor is 72.6.

On the CVC forward branches (Fig. 2), 4 sections can be distinguished, which are approximately approximated by straight line segments, that indicates the manifestation of several different mechanisms of charge carrier transport (current transfer) during forward bias.

Section 1 of the CVC forward branches (Fig. 2) can be represented by an exponential dependence, which is characteristic of the barrier structure:

$$J \propto \exp\left(\frac{qU}{nkT}\right), \tag{2}$$

where q — elementary charge, n — nonideality factor, k — Boltzmann constant [14]. Within the entire studied temperature range $n \approx 2$, therefore, in the section 1 of the CVC forward branches, the electric current is determined by carrier recombination in the space charge region.

Section 2 of the CVC forward branches can be described by the space-charge limited current (SCLC) model, which is characterized by the dependence

$$J \propto U^m, \tag{3}$$

where m – is the exponent characterizing the slope of the corresponding CVC section [15]. In the temperature range 70−250 K $m > 2$, that from the point of view of SCLC model indicates the influence of traps with exponential activation energy distribution [15] on current transfer processes. At $T = 260$−290 K $m = 2$, that is within the limits of SCLC model, according to [15], corresponds to the so-called quadratic trap law and characterizes the influence of a monoenergetic deep center (trap) on the current transfer processes. In the temperature range 300−370 K, the condition $1 < m < 2$ is fulfilled in the section 2 of the CVC forward branches (Fig. 2). According to the SCLC model this means, that the concentration of injected charge carriers becomes comparable with the concentration of charge carriers thermally generated from traps [15].

In segments 3 and 4 of CVC forward branches (Fig. 2) there is a weak $d(\ln J)/dU$ dependence of temperature. This indicates the dominance of the current transfer tunnel mechanism [16]. According to [17], the tunneling of charge carriers can occur inside the *por*-Si film between the energy levels of traps on the surface of silicon crystallites through SiO_x barriers. The difference in the slopes of CVC sections 3 and 4 (Fig. 2) may indicate the influence of groups of traps with different activation energies on the tunneling processes.

The reverse CVC branches, shown in Fig. 3 on a linear scale, are qualitatively characteristic of barrier structures with the so-called „soft“ breakdown [18]. In the reverse bias region, a weak temperature dependence of J is observed at $U \leq 5$ V, that also indicates the tunneling of charge carriers. Thus, according to [18], the form of CVC reverse branches is determined by the competition between

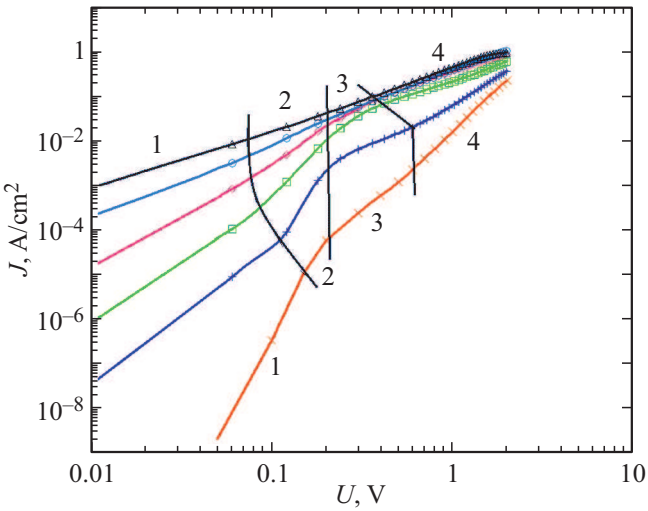

Figure 2. CVC forward branches at temperature T, K: × — 70, + — 140, □ — 200, ◊ — 250, ○ — 300, △ — 370.

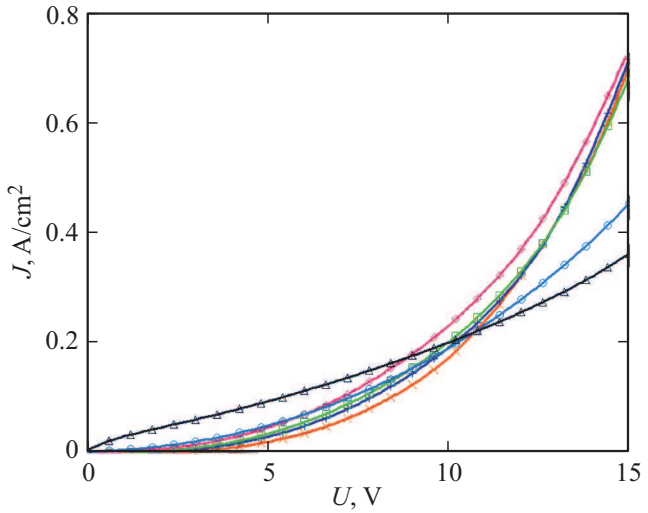

Figure 3. CVC reverse branches at temperature T, K: × — 70, + — 140, □ — 200, ◊ — 250, ○ — 300, △ — 370.

avalanche and tunnel breakdown involving traps with a continuous range of activation energies.

Figure 4 shows the graphs of the temperature dependence of the current density for different values U for forward and reverse bias, as well as at $U = 0$ V. The temperature dependence $J(U = 0\,\text{V})$ was obtained by extrapolation of the CVC forward branches to the indicated value U. At $U = 0$ V the energy of traps activation changes within 0.077−0.212 eV (Fig. 4). In the forward bias region at $U = 0.1$ V, the activation energy change range is 0.061−0.181 eV, at $U = 0.3$ V the range shifts to smaller values 0.008−0.073 eV. The observed decrease in the activation energy with increasing U can be explained by the specificity of the traps distribution, which is typical of surface states on silicon crystallites in the *por*-Si film. At $U = 1$ V (forward bias) in the region of high and low

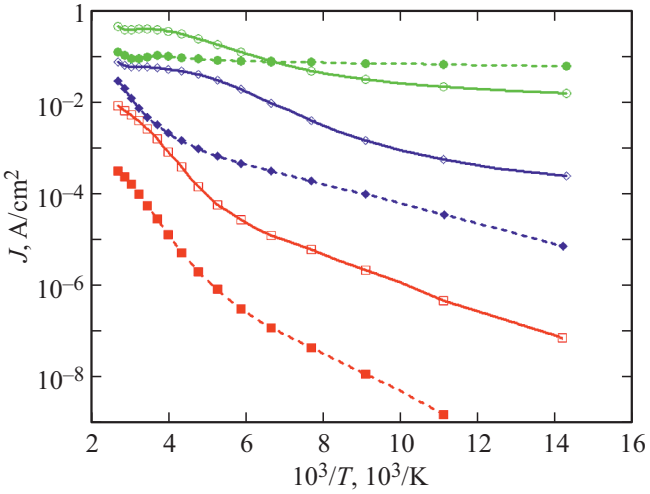

Figure 4. The current density dependence of temperature at $U = 0$ V (■), as well as at forward bias for values U, V: □ — 0.1, ◊ — 0.3, ○ — 1.0 and at reverse bias for the values U, V: ♦ — 1.0, ● — 7.0.

temperatures (Fig. 4) J weakly depends on temperature, that may be due to the absence of the effect of trap recharging on current transfer processes, or to a decrease in potential barrier height, which accompanies the effect of charge carrier tunneling. In the reverse bias region at $U = 1$ V, the states with activation energy in the range of 0.045–0.254 eV are electrically active, that can also be explained by the influence of surface states (Fig. 4). At $U = 7$ V in the reverse bias region (Fig. 4) J weakly depends on temperature, that can also be explained by the absence of traps influence on current transfer processes or by the effect of charge carrier tunneling.

3.3. Results of experimental samples study by the method of current deep-level transient spectroscopy

When measuring the I-DLTS spectra, the traps were filled with a voltage pulse with an amplitude of 0 V, and the DL were emptied at a reverse bias voltage of 2 V. In such a regime, the DL traps of the main charge carriers — holes are predominantly filled. The measurement mode is selected on the basis of the restriction on the maximum possible value of the reverse leakage current through the sample for the used I-DLTS spectrometer [9].

The I-DLTS spectra measured at relaxation times τ 0.46, 0.91, and 1.41 ms are shown in Fig. 5. The spectrum contains DL H1 peak with an activation energy $E_t = 0.46$ eV, which was determined on the basis of inclination of Arrhenius line. The concentration of the traps with DL H1, determined on the peak height in accordance with the method proposed in [19], was $1.37 \cdot 10^{16}$ cm^{-3}. On the I-DLTS spectrum from the low temperature side, there is a broadened „shoulder" in the temperature range 130–205 K, the position of which is almost independent of the time constant τ (Fig. 5). This is typical for a sample with a high density of surface states [20]. In accordance with the method proposed in [20], it was found, that the observed surface states are characterized by an activation energy range of 0.23–0.35 eV, the value of states density is $4.96 \cdot 10^{11}$ cm^{-2}. The observed surface states and DL H1 in the semiconductor structure under study are traps for the major charge carriers — holes. It is important to note, that the concentration of DL H1 and the density of surface states are comparable with the concentration of a fine acceptor impurity ($1.5 \cdot 10^{16}$ cm^{-3}) in a silicon wafer. The region at $T > 300$ K, where the growth of I-DLTS signal is observed, is explained by a sudden increase in the reverse leakage current, against which it becomes impossible to distinguish the current relaxation signal. The change in the intensity of the I-DLTS signal with a change in τ in Fig. 5 is related to the temperature dependence of the maximum amplitude of the relaxation current in the diode structure, in which the concentration of traps is commensurate with the concentration of the major charge carriers.

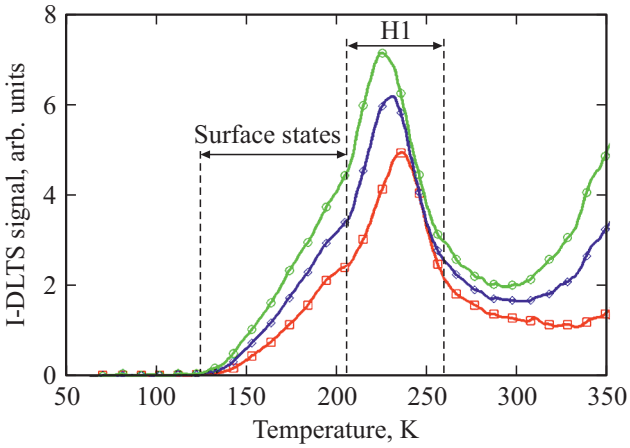

Figure 5. I-DLTS spectra of the experimental sample at time constants τ, ms: □ — 0.46, ◊ — 0.91, ○ — 1.41.

3.4. Discussion of the experiment results

By measuring the thermo-emf sign, it was established that the *por*-Si film of the semiconductor structure under study has the *p*-conductivity type. The silicon substrate also has *p*-conductivity type. The indium contacts to the substrate and *por*-Si film are non-rectifying (ohmic). Studies of the RSS spectra showed, that the dimensional effect is not observed in the silicon crystallites of the *por*-Si film. Therefore, the band gap of *p*-Si substrate and *por*-Si film crystallites is the same. Based on these considerations, the CVC branches under forward and reverse bias should be symmetrical, as a result of which the semiconductor structure under study should not exhibit rectifying properties. At the same time the studies have shown, that in the forward bias there is a CVC section described by formula (2), which is typical of barrier structures with a rectifying effect.

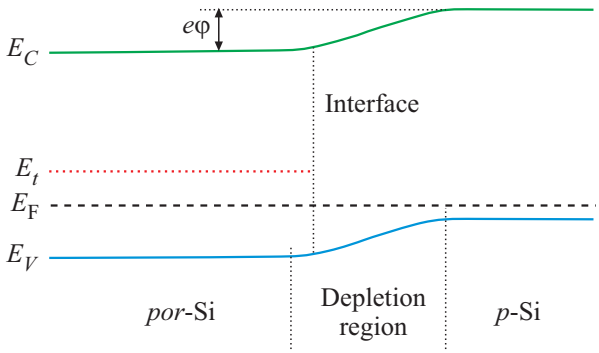

Figure 6. The energy band diagram model of a rectifying junction *por*-Si/*p*-Si.

To explain the current transfer processes in the semiconductor structure under study, we can propose an energy band diagram model for the equilibrium case in the form of Fig. 6.

During the formation of the *por*-Si film, a region with a high concentration of defects appears, which is comparable to the concentration of a small dopant in the original *p*-Si wafer used as a substrate. As was found by measuring I-DLTS spectra, there are surface states at the *por*-Si/*p*-Si interface, as well as a discrete DL H1. The presence of mechanical stresses [21] in *por*-Si, which were found in the course of study of RSS spectra can indirectly contribute to the appearance of defects with DL in *por*-Si film silicon crystallites. The mentioned region may be a partially compensated semiconductor. As a result, at the boundary between *por*-Si and *p*-Si, the Fermi level can be fixed from the *por*-Si side. The space charge region (SCR) of the structure under study is located in *p*-Si. The direction of band bending in the SCR shown in Fig. 6 is due to the presence of the rectification effect [14]. The bending of the bands in Fig. 6 is determined by the barrier height $e\varphi$. When a reverse bias voltage is applied, the value $e\varphi$ increases by U. For forward bias $e\varphi$ decreases. These circumstances can explain the rectifying properties of the semiconductor structure under study.

As a result of the study of the CVC temperature dependence, it was found, that the processes of current transfer are complex. Under forward bias, the processes of charge carrier recombination in the SCR of the semiconductor structure under study predominate, the SCLC mechanism and tunneling of charge carriers inside *por*-Si film between the energy levels of traps on the surface of silicon crystallites also appear through SiO_x barriers. Under reverse bias, the breakdown of the barrier structure occurs, which is determined by the competition between the avalanche and tunnel mechanisms with the participation of traps. Both with forward and reverse biases, current transfer processes are affected by traps with DL, with an activation energy distributed over a wide range of values.

4. Conclusion

It is shown that a structure with a *por*-Si film grown by metal-stimulated etching using silver particles on single-crystalline silicon wafer of *p*-type, has rectifying properties. Since the phonon confinement effect was not observed in the crystallites of the porous film, this means, that there is no dimensional effect in the *por*-Si film, as well as the coincidence of the values of the band gap *por*-Si and single-crystalline *p*-Si. The rectifying properties of the *por*-Si/*p*-Si semiconductor structure can be explained by the presence of a bend in the energy bands due to the fixation of the Fermi level in the *por*-Si layer due to a high concentration of deep centers. The study of the temperature CVC dependence allowed to specify four segments on the forward branch. At low voltages (up to 0.1 B), an exponential dependence of the current due to recombination processes is observed, which is typical of semiconductor barrier structures. As the voltage increases, CVC is described by the current model limited by the space charge. At higher voltages, a weak value dependence of the temperature is observed, that indicates the dominance of the tunneling mechanism of current transfer. The type of reverse CVC branches is determined by the contributions of avalanche and tunnel breakdowns with the participation of traps. The spectra of relaxation spectroscopy of deep levels show peaks corresponding to a deep level with activation energy of 0.46 eV and electrically active surface states with an activation energy range of 0.23–0.35 eV. The observed surface states and the discrete DL in the semiconductor structure under study are traps for major charge carriers — holes.

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Conflict of interest

The authors declare that they have no conflict of interest.

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