MIS transistor based on PbSnTe : In film with an Al_2O_3 gate dielectric*

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Results on the creation and properties of transistor-type MIS structures (MIST) with an Al_2O_3 thin-film gate dielectric based on PbSnTe : In films obtained by molecular beam epitaxy are presented. The source-drain current-voltage characteristics (CVC) and gate-controlled characteristics of the MIST at [B$T = 4.2$ K have been investigated. It is shown that in MIST based on PbSnTe : In films with $n \sim 10^{17}$ cm^{-3} the modulation of the channel current reaches 7–8% in the range of gate voltages $-10\,\text{V} < U_{\text{gate}} < +10\,\text{V}$. The features of the source-drain CVC and the gate-controlled characteristics for a pulsed and sawtooth variation of U_{gate} are considered.

Keywords: solid solution PbSnTe : In, field effect, MIS structure, Al_2O_3.

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1. Introduction

Binary semiconductors PbTe and SnTe form a continuous series of solid solutions $Pb_{1-x}Sn_xTe$ (PbSnTe) in the range $0 \le x \le 1$. A number of interesting properties of PbSnTe, depending on the composition x, are determined by the properties combination of each of these binary compounds. Thus, it is known that PbTe has a normal energy spectrum, while SnTe has an inverted energy spectrum, in which the bottom of the conduction band and the top of the valence band change over. At the inversion point ($x_{\text{inv}} \approx 0.35$ at $T = 4.2$ K) the band gap E_g goes to zero (gapless state), increasing linearly both with x increasing and decreasing with respect to x_{inv}. The composition-controlled small forbidden gap width E_g was the basis for the development in 80s of infrared (IR) photodiodes (PD) based on PbSnTe. The strong effect of surface leakage currents on the IR PD parameters, noted, for example, in [1–3], facilitated the study of surface properties and methods of surface passivation.

It is known that SnTe is a ferroelectric, and PbTe is a virtual ferroelectric. Accordingly, the Curie temperature for different x is different. Besides, the temperature-dependent static permittivity ε also varies strongly with composition change. For PbTe at $T = 80$ K it is $\varepsilon \approx 400$ and significantly increases with x increasing, thus reaching $\varepsilon \approx 2000-4000$ and even > 10000 at high content of SnTe and helium temperatures. Apparently, due to the large value of the static dielectric permittivity a limited number of papers is known relating the properties study of the PbSnTe surface using metal-insulator-semiconductor (MIS) structures and capacitance-voltage ($C-V$) measurements. Thus, in [4] the capacity modulation of MIS structures was observed within the limits of up to several percent, and the contribution of surface traps to the observed features of $C-V$-characteristics was noted. After 1980s, CdHgTe became the main material for IR technology, and interest in studying the properties of the PbSnTe surface with the composition $x < x_{\text{inv}}$, being basis of IR FDs development, practically disappeared.

Another factor that significantly hinders the use of MIS structures for surface studies is the high concentration of free charge carriers $n_0(p_0)$ in undoped PbSnTe. It is due to a high concentration of intrinsic electrically active defects, which create „shallow“ levels in PbSnTe. As a result, there are no data in the literature on reaching the concentration of free charge carriers $n_0(p_0)$ less than $\sim 10^{15}$ cm^{-3} (in n-PbTe) in undoped PbSnTe even at helium temperatures. Close to compositions with $x \approx x_{\text{inv}}$ or $x > x_{\text{inv}}$ the value of $n_0(p_0)$ is, as a rule, higher by 2–3 orders of magnitude. In particular, the corresponding high „bulk“ conductivity even of thin PbSnTe films significantly complicates the study of the transport properties of the surface. However, it is known [5,6] that adding indium to PbSnTe of a certain composition in concentrations up to several at% can reduce $n_0(p_0)$ by several orders of magnitude, and in a narrow range of compositions practically up to its own concentration n_i even at helium temperatures of („insulating“ state). In principle, this ensures opportunities for studying the transport properties of the surface both directly in PbSnTe : In films and in heterostructures based on „insulating“ PbSnTe : In with an upper thin layer with

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the composition of a topological crystalline insulator (TCI), which is realized at $x > x_{inv}$ or near $x \approx x_{inv}$.

Even in the 80s of the last century, the properties of a heterojunction between PbSnTe with „normal“ and „inverted“ spectrum were considered in the paper [7]. It was shown that, in this case, states with a linear dispersion law should be present at the heterointerface. Much later, in a number of theoretical and experimental works (for example, [8–11]), it was shown that in $x > x_{inv}$ region PbSnTe belongs to TCIs in which Dirac states are formed on the surface even without heterojunction. Particular interest in TCI in general and in PbSnTe in particular is associated with the spin properties of such surface states. This ensures potential opportunities for creating spintronic devices based on PbSnTe, in which control of charge flows (electronics) is replaced by control of spin flows. In connection with above said, it is clear that the study and control of PbSnTe surface properties, including its stabilization, is again of particular interest.

In literature there is no data on the study of the field effect in transistor-type MIS structures based on PbSnTe with a thin-film gate dielectric. This can also be due to large values of ε and high bulk conductivity of undoped PbSnTe. The results of studying the field effect in structures based on indium-doped „insulating“ films of PbSnTe : In using a $8\,\mu$m thick Mylar film as a gate dielectric are presented in [12]. It is shown that, at a qualitative level, a number of observed features are associated with surface properties.

The purpose of this paper is to create transistor type MIS structures based on PbSnTe : In films with thin-film gate dielectric, to study and analyze their properties at $T = 4.2$ K.

2. Samples and experimental procedure

The technology for obtaining the initial PbSnTe : In films by molecular beam epitaxy is described, for example, in [13]. Films $1-2\,\mu$m thick were grown on (111) BaF_2 substrates. The films composition after growth was determined by X-ray microanalysis, the concentration and mobility of free charge carriers were estimated from measurements of the Hall effect in a magnetic field $B = 0.2$ T. The paper describes the properties of transistor-type MIS structures made on the basis of film with PbSnTe : In of the electron conductivity type with thickness of $d = 1.3\,\mu$m. The content of SnTe was relatively low and corresponded to $x = 0.163$ at In concentration ~ 0.63 at%. For such compositions, the electron conductivity type is usually realized with a rather high concentration n_0. The electrons concentration and mobility were estimated from the expressions $n_0(T) = -1/qR_H(T)$ and $\mu(T) = -R_H(T)\sigma(T)$. The Hall coefficient $R_H(T)$ and conductivity $\sigma(T)$ were measured using a standard Hall bridge fabricated by photolithography. The concentration n_0 calculated in this way slightly, by maximum 2 times, changed in the range $T = 4.2-100$ K. For $T = 4.2$ K $n_0 = 1.7 \cdot 10^{17}$ cm^{-3}, and the mobility is

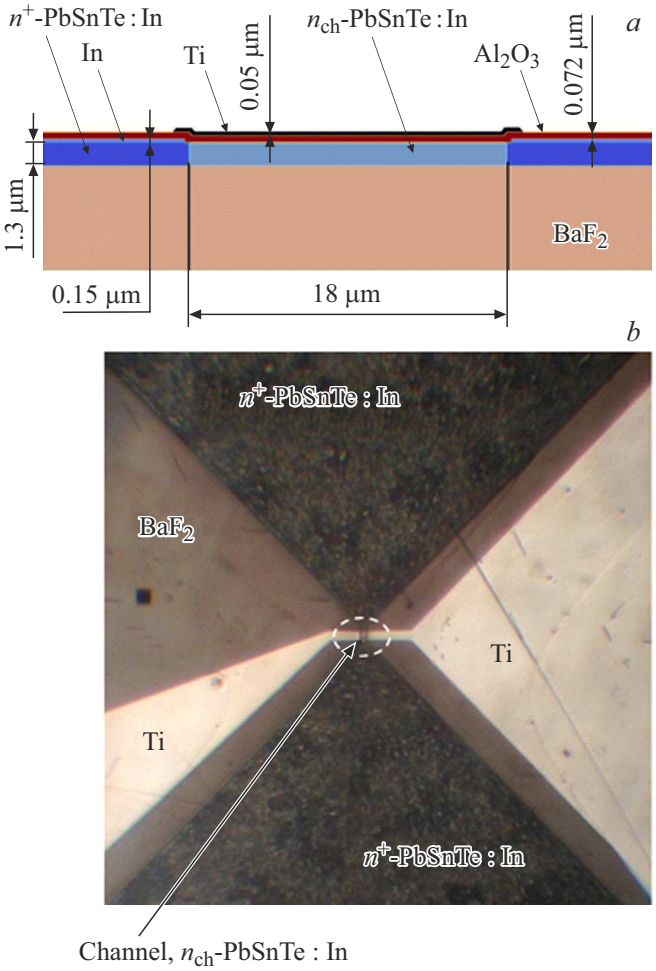

Figure 1. Schematic representation of the transistor-type MIS structure in the section (a) and photo of the finished experimental structure in the vicinity of the channel (b).

$\mu = 3.8 \cdot 10^4$ cm$^2 \cdot$ V$^{-1} \cdot$ s^{-1}. Such mobility values confirm the rather high crystal quality of the film, which is controlled during its growth by reflected high energy electron diffraction (HEED).

Fig. 1 shows a schematic representation and photo of an experimental transistor-type MIS structure in the vicinity of the channel. In Figure n_{ch}-PbSnTe : In is the channel region with properties determined by the properties of the original PbSnTe : In film. The source-drain regions (SDRs) n^+-PbSnTe : In were created by diffusion annealing of an indium layer with a thickness of $\sim 0.15\,\mu$m, which is ~ 0.1 of PbSnTe : In film thickness. The thickness-averaged concentration of indium additionally introduced into the SDRs was ~ 10 at%. A layer of indium was deposited in a vacuum at a temperature of $\sim 120^\circ$C onto a surface covered with a photoresist with windows opened for SDRs. After the photoresist removal and diffusion annealing of indium for ~ 40 min at $T \approx 180^\circ$C the PbSnTe : In film was etched to BaF_2 substrate using photolithography outside the channel and SDRs areas. After that, for the oxides

removal the PbSnTe surface was treated in HCl solution in isopropyl alcohol [14] and after minimal exposure to air (5–10 min), the sample was loaded in Al_2O_3 atomic layer deposition chamber. Al_2O_3 layer 72 nm thick was deposited on the entire surface of the structure. After that, similarly to the procedure for In layer obtaining in SDRs, using vacuum deposition and „explosive“ photolithography a metal gate made of titanium with a thickness of ~ 50 nm was formed over the channel area. Windows in Al_2O_3 were not opened for contacts to SDRs. Such contacts were created by soldering thin silver wires with indium using a microsoldering iron in regions $\sim (0.1-0.2)\,\mathrm{mm}^2$. These areas were chosen far from the location of the channel, and a thin layer of Al_2O_3 in these areas was specially destroyed mechanically with the microsoldering iron. The quality of the contacts to SDRs obtained in this way was checked by measuring the resistance between the source and the drain. Besides, a specially chosen large size of SDR ($\sim 1 \times 1\,\mathrm{mm}^2$) on MIS structures made it possible to use the Van der Pauw method to check SDR parameters. In this case, four contacts were created along the edges of the SDR in the corresponding places.

With the procedure used for creating MIS structures, „a step“ with a height close to the thickness of the initial PbSnTe : In film, i.e. $\sim 1.3\,\mu$m, appears in the channel region. At this step, in principle, the Ti layer and, accordingly, the gate circuit can break. To check the break absence two contact pads were created to the Ti-gate (to the right and left of the channel in Fig. 1). This allowed us to check the absence of breaks by the resistance between two Ti-pads. Testing at room temperature showed that the gate circuit had no breaks in any of the 6 MIS structures tested. At the same time, the leakage current through the gate Al_2O_3 in all 6 structures did not exceed 10^{-11} A (the lower limit of measurements of ammeter used for testing) at gate voltage up to ± 10 V. Note that the leakage currents through the gate dielectric in the samples of transistor-type MIS structures studied at $T = 4.2$ K did not exceed the measurement accuracy, which was better than 10^{-12} A.

When measuring the current–voltage characteristics (CVCs) and gate-controlled characteristics of structures at helium temperatures the standard instruments and procedures were used. The samples were placed directly in liquid helium in a metal chamber that shielded the samples from background radiation.

3. Experimental results

3.1. Current-voltage characteristics of channel of transistor-type MIS structures

The temperature dependence of the resistance „per square“ $R_\square(T)$ and the electrons concentration in the DRS of the structure were measured by the Van der Pauw method. $R_\square(T)$ value monotonically decreased from room temperature to $T = 4.2$ K and had a characteristic break near the temperature $T \approx 7$ K, above which

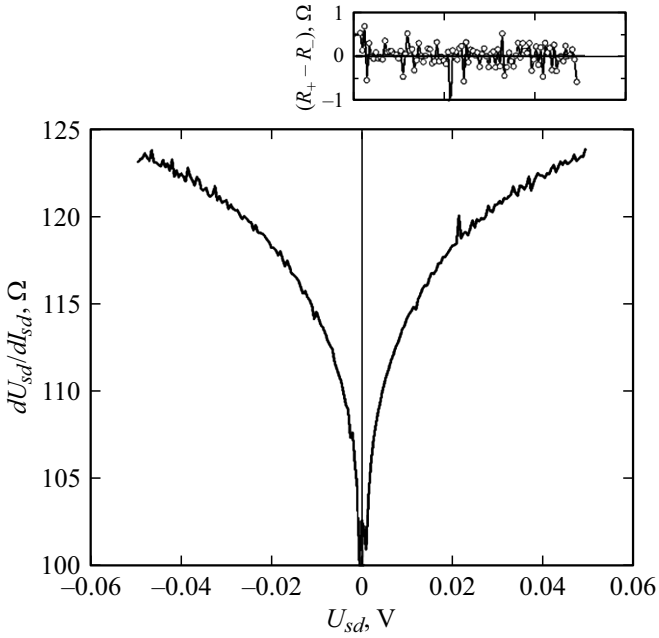

Figure 2. Numerically calculated from CVC the dependence of differential resistance of transistor-type MIS structure $R = dU_{sd}/dI_{sd}$. Top — difference $(R_+ - R_-)$ between differential resistance at $U_{sd} > 0$ and at $U_{sd} < 0$ with equal absolute values U_{sd}.

$R_\square(T) \approx 9$ Ohm, and below $R_\square(T)$ it decreased much faster, reaching $R_\square(T) \approx 2.3$ Ohm at $T = 4.2$ K. This value by an order of magnitude or more is below the channel resistance of the MIS structure and has little effect on the shape of the channel CVC. At $T = 4.2$ K the concentration is $n_0 \approx 6 \cdot 10^{17}\,\mathrm{cm}^{-3}$, and the electrons mobility is $\mu \approx 4.5 \cdot 10^4\,\mathrm{cm}^2 \cdot \mathrm{V}^{-1} \cdot \mathrm{s}^{-1}$. In this case, in Fig. 1, *b* macroscopic inhomogeneities in the SDR are clearly visible, the characteristic size of which is $\sim (10-100)$ nm.

The measured source-drain CVC slightly differs from the linear one and is symmetrical with respect to the sign of the source-drain voltage U_{sd}. This is clearly seen from Fig. 2, which shows the differential resistance $R = dU_{sd}/dI_{sd}$ vs. source-drain voltage. The maximum value U_{sd} was limited due to the possible heating of the channel of the transistor-type MIS structure by Joule heat with a power of $P = U_{sd}I_{sd}$. The channel area was $S_{\mathrm{ch}} \approx 1.8 \cdot 10^{-6}\,\mathrm{cm}^2$, at $U_{sd} = 0.05$ V current $I_{sd} = 4 \cdot 10^{-4}$ A and $P/S_{\mathrm{ch}} \approx 1\,\mathrm{W} \cdot \mathrm{cm}^{-2}$. The absence of CVC significant deviations from linearity at the maximum $U_{sd} = 0.05$ V makes it possible to consider the heating of the structures at such a power to be insignificant. This is ensured by a sufficiently high thermal conductivity of the BaF_2 substrate of millimeter dimensions, cooled by liquid helium and acting as a „heat sink“ for the channel of the transistor-type MIS structure of micrometer dimensions (Fig. 1, *b*). In Fig. 2 one can clearly see the CVC high symmetry with respect to the polarity U_{sd}. The upper part of the Figure additionally shows the dependence

$(R_+ - R_-) = f(U_{sd})$, where R_+ and R_- are differential resistances for positive and negative U_{sd} with the same absolute value. The average value of $(R_+ - R_-)$ over the entire range U_{sd} was 0.0083 Ohm with a standard deviation of 0.28 Ohm, only.

In principle, the total differential conductivity of the channel $\Sigma_{ch} = 1/R$ can be represented as $\Sigma_{ch} = \Sigma_1 + \Sigma_2$, where Σ_1 is ohmic conductivity „of the bulk“ of the channel, while Σ_2 is monotonically and sublinearly decreasing with U_{sd} increasing, and tending to saturation conductivity of some additional channel, possibly connected with the surface.

3.2. Gate characteristics

Fig. 3 shows source-drain current $I_{sd}(t)$ vs. time in the channel of the transistor-type MIS structure at $U_{sd} = 0.01$ V and the corresponding dependence $U_{gate}(t)$. It can be seen from the Figure that the modulation I_{sd} by the gate voltage U_{gate} is $\sim 7\,\mu$A, or (7–8)%. After U_{gate} „step“ switching with a rapid change of I_{sd} value, its slow relaxation is observed for tens of seconds or more, which is not exponential. At the same time, in the region of „the step“ on U_{gate} the characteristic switching times do not exceed several milliseconds. It can be seen that after switching from $U_{gate} = -10$ to $+10$ V near $t = 18.8$ s, the current relaxation differs markedly from its relaxation near $t = 128.5$ s, where the gate voltage was switched from $U_{gate} = 0$ to -10 V. These relaxation dependences are combined in Fig. 4. Curve *1* corresponds to the moment $t_0 = 18.8$ s, curve *2* — to $t_0 = 128$ s; for the curve *1* the function $F(t) = (I_{sd} - I_0)/(I_{sd} - I_0)_{max}$, $I_0 = 9.339 \cdot 10^{-5}$ A, for the curve *2* the function $F(t) = (I_0 - I_{sd})/(I_0 - I_{sd})_{max}$,

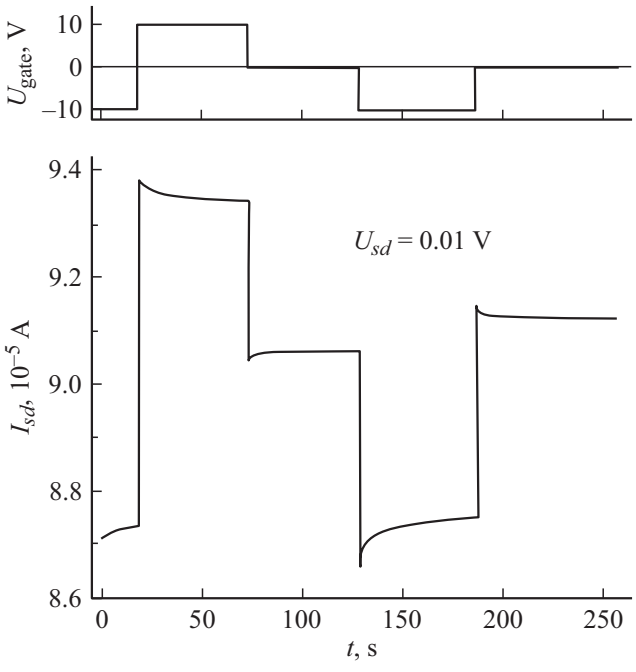

Figure 3. Current through channel of the MIS transistor $I_{sd}(t)$ vs. time, and the corresponding dependence $U_{gate}(t)$ at $U_{sd} = 0.01$ V.

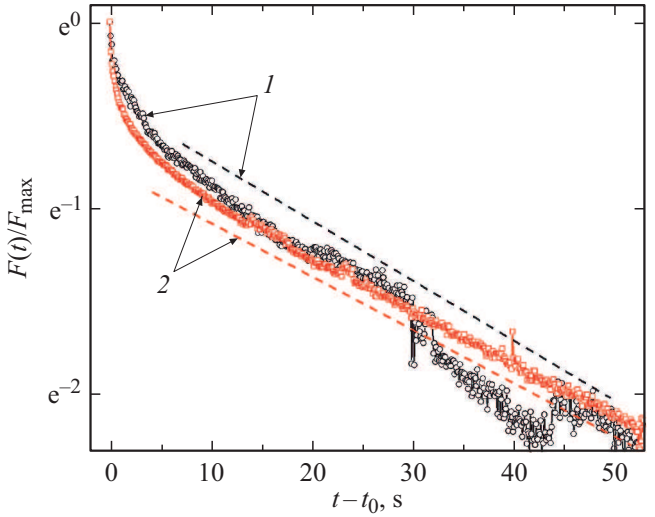

Figure 4. Combined relaxation dependences in semilogarithmic scale. *1* — switching U_{gate} at time $t_0 = 18.8$ s, *2* — at time $t_0 = 128$ s. Dashed lines are exponential dependences with time constant 31 (*1*) and 36 s (*2*). See text for explanation.

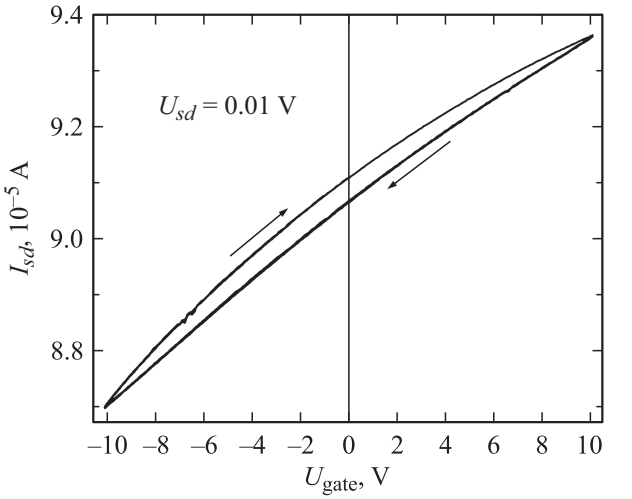

Figure 5. Gate characteristic with a sawtooth change U_{gate} with a sweep period 200 s is $U_{sd} = 0.01$ V.

$I_0 = 8.758 \cdot 10^{-5}$ A. I_0 values represent the current I_{sd} at $t \to \infty$. At the same time, for *2* the value $(I_0 - I_{sd})_{max} = 9.584 \cdot 10^{-7}$ A by more than two times exceeds $(I_{sd} - I_0)_{max} = 4.343 \cdot 10^{-7}$ A for the dependence *1*. It can be seen from the Figure that at the initial moment *2* curve falls noticeably faster than *1* curve, and then after 10–20 s, on the contrary, *1* curve decreases faster. You can also see a noticeable difference in direct current at $U_{gate} = 0$ in the range $\sim (73–128)$ s and in the region $t > 188$ s.

Figure 5 shows the gate-controlled characteristic of the transistor-type MIS structure at $U_{sd} = 0.01$ V, measured upon sawtooth change of U_{gate} in the range ± 10 V with a period of 200 s. Two periods are shown. It can be seen

that the dependence $I_{sd} = f(U_{\text{gate}}$, which has a pronounced hysteresis, is well reproduced. The hysteresis value is $\sim 7\%$ at $U_{\text{gate}} = 0$ with respect to the difference between the maximum and minimum currents in the Figure. The characteristic shape of the dependence and the hysteresis value weakly depend on U_{sd}.

4. Discussion of results

The most important experimental result, in our opinion, is the very fact of observing a rather strong current modulation in the channel of the transistor-type MIS structure based not on „insulating“ but on a „conductive“ PbSnTe : In film. We will focus on a qualitative analysis of the results obtained within the framework of a simplified model. Its main provisions can be formulated as follows. First, we assume that the electric field of the gate weakened at the PbSnTe : In/Al_2O_3 interface by $k_\varepsilon = \varepsilon(\text{PbSnTe})/\varepsilon(Al_2O_3)$ times is completely screened at PbSnTe : In film thickness by induced free (responsible for changing the channel conductivity) and localized charge, including the charge at the PbSnTe : In/Al_2O_3 interface. For simplicity, assume that the induced charge is uniform over the channel area. Also assume that n^+-SDR formed during formed during structure fabrication provide ohmic resistance at the interface with the channel.

In the experiment, with the thickness of the gate Al_2O_3 $d(Al_2O_3) = 72\,\text{nm}$, the maximum value of the field in the dielectric (positive and negative) was $E_{\text{gate}} = 1.4 \cdot 10^6\,\text{V/cm}$. For alumina the low-frequency $\varepsilon(Al_2O_3)$ depends on the preparation method, thickness, and not too strongly depend on temperature (see, for example, [15]). In our experiment, it was not measured, so for estimates we take the value $\varepsilon(Al_2O_3) = 10$, which is close to the data of [15]. In papers [16,17] the value of ε(PbSnTe) for our films with $x = 0.26$ was estimated to be $\sim (2000-3300)$. For estimates, we take $\varepsilon(\text{PbSnTe}) = 2000$. Then $k_\varepsilon = 200$, and the maximum value of the electric field in the PbSnTe : In film at the interface with Al_2O_3 in this case will be $E_{\text{gate}} = 7 \cdot 10^3\,\text{V/cm}$. From the ratio $\varepsilon\varepsilon_0 E = \sigma_s$, where σ_s is the charge surface density, it follows that the electric field of this magnitude will be screened by the charge of electrons (holes) with surface density $N_{sg} = 3.87 \cdot 10^9\,\text{cm}^{-2}$. When the sign of U_{gate} with the maximum value $U_{\text{gate}} = 10\,\text{V}$ changes, the change in density will be $N_{sg} = 7.74 \cdot 10^9\,\text{cm}^{-2}$. In the limiting case, for example, in the absence of a localized charge or immediately after U_{gate} rapid change, all this charge falls on free carriers. In Fig. 3, 5, the change in the channel current when U_{gate} changes by 20 V reaches $\sim (7-8)\%$. Taking into account the thickness of the initial film and the concentration of electrons in it (Sec. 2), at $U_{\text{gate}} = 0$ the surface density of electrons in the film is $N_s \approx 2 \cdot 10^{13}\,\text{cm}^{-2}$. If we assume that the charge carriers screening the field have the same mobility as the electrons in the initial film, then $\delta N_{sg}/N_s = 3.87 \cdot 10^{-4}$, or 0.0387%. This value is by ~ 180 times less than that observed in the experiment. In principle, this discrepancy can be explained by the significant difference between the properties of the near-surface region of PbSnTe : In, in which field screening occurs, and the properties of film „bulk“ namely, the high mobility μ_s of charge carriers (electrons) in it and (or) much smaller ε(PbSnTe) in this layer, for example, due to the difference in the composition of the near-surface region from the film „bulk“. This may be due to the features of the technological modes of film growth. Assuming that ε(PbSnTe) is equal in thickness, we obtain the value of „surface“ mobility $\mu_s = 5.4 \cdot 10^6\,\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$, which looks unlikely. It can be assumed that, nevertheless, there is simultaneously and significantly greater mobility μ_s compared to „bulk“ mobility, and a smaller value of ε in the near-surface layer compared to „bulk“. In any case, the obtained value of the current modulation by the gate voltage can be explained only on the assumption that the properties of the near-surface layer differ significantly from the properties of the film „bulk“. On a qualitative level, this assumption is consistent with the rather unusual source-drain CVCs (Fig. 2), which can be explained by the presence of conductivity connected in parallel with the bulk conductivity and dependent on the source-drain voltage. In view of the foregoing, this part of the conductivity can be associated with the near-surface region.

Within the framework of the simplified model the relaxations I_{sd} in Fig. 3 and hysteresis in Fig. 5 are explained as follows. Immediately after switching from $U_{\text{gate}} = -10\,\text{V}$ to $+10\,\text{V}$ near $t = 18.8\,\text{s}$, the electric field is screened only by nonequilibrium mobile electrons and I_{sd} is maximum. After that, the capture of electrons by traps begins at a constant value of the total „induced“ near-surface charge with the density decreasing of free electrons. As a consequence, the current decreases down to $t \approx 73\,\text{s}$. Further, when the gate voltage is switched to $U_{\text{gate}} = 0$, a small „dip“ in I_{sd} value is observed. It is explained by the fact that electrons captured by slow traps create a negative electric field. As they are depleted in the region $t \approx 73-128\,\text{s}$, the indicated field decreases with slow I_{sd} increasing. After applying $U_{\text{gate}} = -10\,\text{V}$ to the gate at $t \approx 128\,\text{s}$, the field is screened at the first moment only due to a change (decreasing) in the density of electron mobile charges and I_{sd} minimum („dip“) is observed. After the subsequent slow ionization of slow traps, the density of mobile electrons increases, and I_{sd} increases up to $t \approx 188\,\text{s}$. After switching to $U_{\text{gate}} = 0$ at the time $t \approx 188\,\text{s}$ the deep traps remain partially ionized compared to the equilibrium state, creating a positive electric field. This explains I_{sd} „surge“ and the subsequent slow decreasing of the current due to the traps filling with electrons. These processes are also associated with the current difference in the intervals $t \approx 73-128\,\text{s}$ and $t > 188\,\text{s}$, in which $U_{\text{gate}} = 0$. In the first one, „discharging“ of deep traps occurs, which captured electrons and create negative field, in the second interval electrons are captured by ionized traps, which create a positive field. In our opinion, it is difficult to conclude from the results presented whether the formation of „slow“

negative and positive charges occurs due to the recharging of the same traps or different ones. On the one hand, the difference between the curves in Fig. 4 (*1* — capture, *2* — ejection of electrons from traps according to the model) speaks in favor of different types of traps for electrons and holes. At the same time, the difference between the curves in Fig. 4 is not too strong, and the characteristic times of electrons capture and ejection can also differ for one type of traps. At the same time, the shown non-exponential nature of the relaxation processes suggests that, as in the insulating PbSnTe : In films, there is an traps distribution by energy, this was shown in [18–20]. The hysteresis in Fig. 5 is also qualitatively described by the formation of „slow“ negative surface charge of traps with $U_{\text{gate}} > 0$ increasing, which remains significant even after decreasing, and even U_{gate} sign change. On the contrary, $U_{\text{gate}} < 0$ forms a slowly varying positive charge associated with decreased traps filling with electrons compared to the equilibrium case.

5. Conclusion

As a result of the studies carried out on the basis of PbSnTe : In films obtained by molecular beam epitaxy, for the first time in the world experimental samples of transistor-type MIS structures with thin-film gate dielectric were developed and manufactured. 72 nm thick Al_2O_3 layer with an electrical strength of at least $1.5 \cdot 10^6$ V/cm and leakage currents 10^{-12} A maximum at gate voltage $U_{\text{gate}} = 10$ V was used as such dielectric. At $T = 4.2$ K the source-drain CVC and current modulation in the channel of the transistor-type MIS structure based on PbSnTe : In film with the electrons concentration $\sim 10^{17}$ cm^{-3}, which, when the gate voltage changed within the range up to $U_{\text{gate}} = \pm 10$ V, reached 7–8%. A joint analysis of CVC and gate-controlled characteristics shows that the results obtained can be explained by the difference between the parameters of the near-surface layer of PbSnTe : In film and „bulk“ with increased electrons mobility and, possibly, with reduced static dielectric permittivity. The observed slow relaxations of the channel current are explained by the slow traps presence near the PbSnTe : In surface, which may be distributed by energy in the forbidden band. To refine the model of real MIS transistor, additional studies are required.

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Conflict of interest

The authors declare that they have no conflict of interest.

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