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The Effect Of A Strong Static Electric Field And Heating On Characteristics Of The High-Frequency Impedance Of Metal–Ferroelectric–Semiconductor Structures

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Studies have been carried out on the effect of heating and a strong field, but pre-breakdown, effects on high-frequency characteristics of the impedance of heteroepitaxial structures Ni−$Ba_{0.8}Sr_{0.2}TiO_3$−*p*Si with a ferroelectric thickness of 50 nm. It was shown, that regardless of the polarity of the field stress, characteristics shifted towards a positive bias, and the width of hysteresis loops decreased; plateau levels remained virtually unchanged. Heating up to 121°C led to a change in levels of the upper plateau of characteristics: for the capacity it decreased, and for the conductivity it increased; branches on the loop not only narrowed and shifted, but changed places in comparison with the original dependence (loop reverse). These results can be explained: under the field action, by the generation of additional electronic states, localized in the buffer layer at the Si−$Ba_{1-x}Sr_xTiO_3$ interface, and by heating, by the appearance of delay effects due to the development of fluctuation processes, underlying the smearing of the phase transition from ferroelectric to paraelectric condition.

Keywords: High-frequency field characteristics of the impedance, the field stress, hysteresis loops, the generation of additional localized electronic states, delay effects, fluctuation processes, smearing of the phase transition.

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1. Introduction

One of the priority lines of silicon oxide alternative investigations includes the use of ferroelectric films as insulating layers for nanoscale electronic devices [1]. The unique physical properties of ferroelectric materials (in particular, high permittivity adjustable by an external electric field) make it possible to make basically a brand-new class of data storage and processing devices based on the planar technology [2]. Barium-strontium titanate ($Ba_{1-x}Sr_xTiO_3$ or BST) solid solutions are promising ferroelectric compounds for microwave technology applications [1,2]. They have ferroelectric properties at temperatures above room temperature and effective permittivity of their thin films remain at the highest ever level (by a factor of hundreds higher than that of SiO_2) in a wide temperature range. Control actions on ferroelectric layers in micro- and nanoelectronic devices are accompanied by significant electric displacements which are applied to the depth of a sample and induce BST field equal to several MV/cm. Such loads cause structure damage, which is named similar to silicon items, when the high frequency impedance characteristics change after field or high-temperature exposure and then recover back to their initial state after about 24 hours. Also, similar to silicon-based structures, terms field stress and temperature (thermal) stress will be used for such actions. Currently, there are scarcely any publications devoted to the investigation of electrophysical property variation patterns in metal−BST−Si structures after field and thermal exposure. There is a considerable gap in knowledge of BST ferroelectric resistance to field and thermal loads. Therefore, an important research area includes the investigation of property change patterns of metal−BST−Si structures that do not result in breakdown-type damage after field and thermal stresses. This issue is discussed herein using metal−BST−*p*Si structures with ferroelectric layer thicknesses of 50 nm.

2. Influence of stresses on the high frequency impedance of Ni−$Ba_{0.8}Sr_{0.2}TiO_3$−Si structures

The experimental investigations have been carried out on heteroepitaxial Ni−$Ba_{0.8}Sr_{0.2}TiO_3$−*p*Si structures with a nickel field plate area of $S = 2.7 \cdot 10^{-4}$ cm^2. A $h = 50$ nm thick ferroelectric film was deposited by the polycrystalline target HF sputtering in oxygen atmosphere using Plazma-50SE system (Russia). For more details of the system design and the film deposition technique,see [3,4]. Impedance measurements were carried out in the range from room temperature to 121°C at 1 MHz using LCR Agilent E4980A precision meter, a laptop with updated software, and a special camera furnished with a heating

table with thermal stabilization. For more details of the experimental system, see [5]. A bias voltage V_g from -8 V to $+8$ V with 0.005 V increment and sensing signal amplitude 25 mV with a reading rate of 3 points per second was supplied to the metal-ferroelectric–semiconductor structure.

The samples were held during 30 min. at room temperature and constant voltages from ± 2 to ± 8 V to ensure the field stress exposure range. Thermal stress for achieved by heating of the sample up to 121°C and by high frequency measurements at this temperature. The experimental results are shown in Fig. 1–4.

Field stress caused obvious changes in the high frequency impedance curves. Both at negative and positive stress voltages, curve shifts towards positive bias and reduction of the hysteresis loop widths were observed (see Fig. 1, 2). However, the curve plateau levels remain almost unchanged. The effect of positive-polarity strong electric field exposure on both high frequency capacity

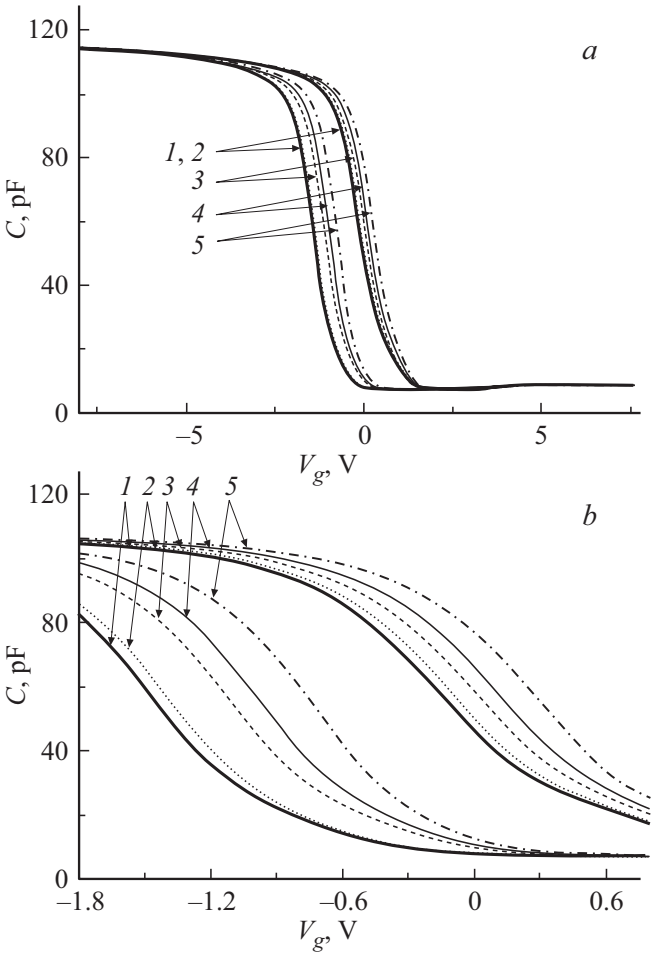

Figure 1. Changes in capacity-voltage curves of Ni–$Ba_{0.8}Sr_{0.2}TiO_3$–Si structures after field exposures with various amplitudes: *a* — main view of the curves, *b* — scaled-up view of the hysteresis loop. Curve Nos.: *1* — initial, *2* — after -4 V stress, *3* — after -8 V stress, *4* — after $+4$ V stress, *5* — after $+8$ V stress.

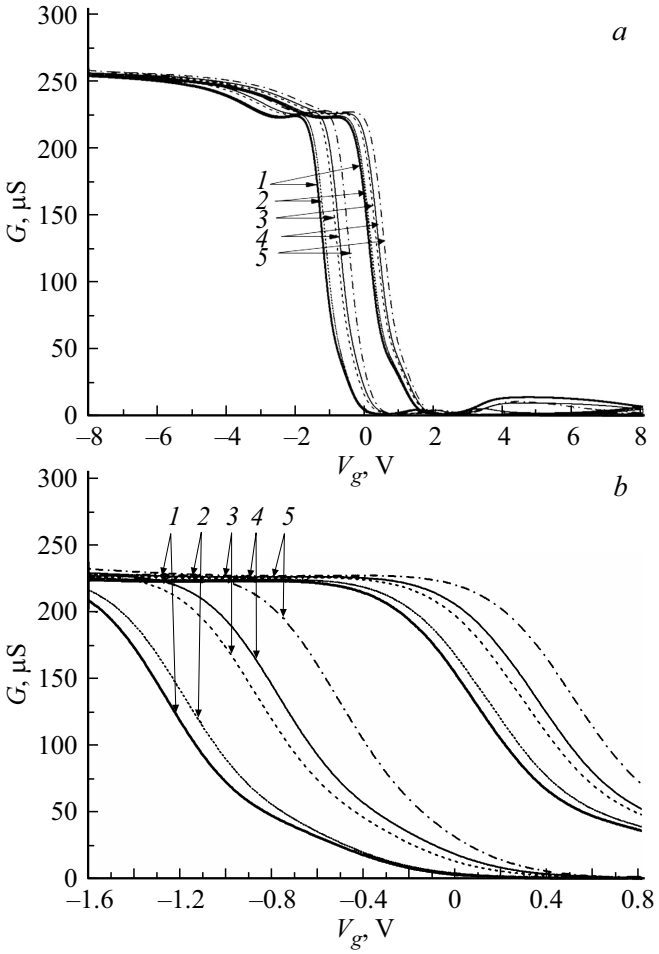

Figure 2. Influence of the field stress on the conductivity curves of Ni–$Ba_{0.8}Sr_{0.2}TiO_3$–Si structures. *a* — main view of the curves, *b* — scaled-up view of the hysteresis loop. Curve Nos.: *1* — initial, *2* — after -4 V stress, *3* — after -8 V stress, *4* — after $+4$ V stress, *5* — after $+8$ V stress.

and conductivity was greater than the effect of negative polarities. The Table shows the experimental data of changes in voltage-capacitance curves after various field stresses.

The thermal stress caused greater changes in high frequency impedance response than the field stress, see Fig. 3, 4. The curves not only shifted, but also the upper plateau level was changed: decreased level for capacity, and increased level for conductivity. The branches of the curve loop measured at 121°C were not only narrower, but swapped with each other compared with the initial curve, see Fig. 3 (loop reverse).

3. Discussion

Similar to traditional metal–SiO_2–Si structures, the high frequency impedance change pattern of metal–ferroelectric–semiconductor samples after long-term holding in strong electric field may be explained by formation of locali-

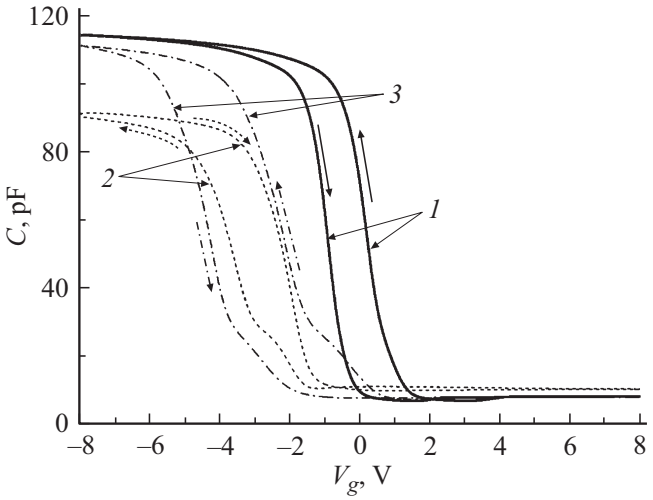

Figure 3. Change in capacitance-voltage curve of $Ni-Ba_{0.8}Sr_{0.2}TiO_3-Si$ structure during heating. Curve Nos.: *1* — initial, *2* — measurements at 121°C, *3* — measurements immediately after cooling down to room conditions.

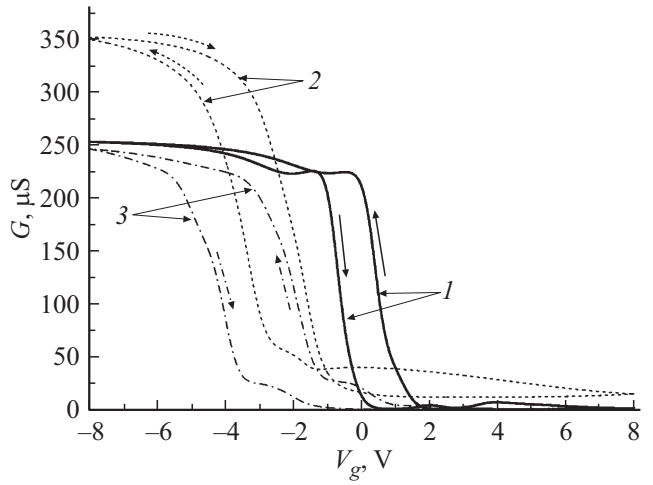

Figure 4. Change in conductivity curves of $Ni-Ba_{0.8}Sr_{0.2}TiO_3-Si$ structure during heating. Curve Nos.: *1* — initial, *2* — measurements at 121°C, *3* — measurements immediately after cooling down to room conditions.

zed electronic states on the BST-silicon interface after stresses [6–8]. This interface is complex and contains a thin (several nm) buffer layer with native silicon oxide to Si. It is known that on the $Si-SiO_2$ interface, there are so called dangling silicon bonds [9] are not only recharged when potential is changed, but their concentration is increased with the strong electric field exposure. Moreover, the number of localized electronic states is increased at both electrical exposure polarities. Experiments described in [10,11] show that due to electron trap recharging in the buffer transition layer between the ferroelectric and semiconductor, the field effect at the BST–Si interface is rather weak. Virtually whole external field is shielded by charges in the transition

Changes in voltage-capacitance curve of the sample after field stress. (Hysteresis loop width and shift were defined at the curve half height at 60 pF. The change in the left branch of the capacity-voltage relationship was assumed as the shift)

	Field exposure				
	Initial, without stress	−4 V	−8 V	+4 V	+8 V
Hysteresis loop width, B	1.32	1.30	1.145	1.11	1.03
Hysteresis loop shift, B	–	0.069	0.37	0.47	0.70

layer, voltage drop across the semiconductor is small, high frequency capacity of the metal–BST–Si structure is governed by silicon and field band bending displaced from the flat band state only by a few kT/q throughout the observed bias range, where k is the Boltzmann's constant, T is the absolute temperature, q is the elementary charge. U-shaped energy density of localized states with minimum in the vicinity of silicon flat bands which is inherent to the high concentration of disordered traps in the buffer layer determines sudden slowing-down of the increase/decrease in the external voltage drop on the semiconductor during enrichment/depletion, respectively. In its turn, this deceleration causes: firstly, appearance of two field plateaus on the metal–BST–Si structure high frequency impedance curves that are not attributable to the strong enrichment or semiconductor surface inversion in any way, and secondly, hysteresis loop arrangement on these curves in the vicinity of the semiconductor flat band states. The first exposure causes the increase in the energy density of electronic states localized in the transition layer and their charge modulus is increased. Accordingly, at the same bias, the absolute charge of the semiconductor surface region associated with free carrier flow for the external field shielding shall be reduced. Thus, the band bending modulus in silicon is reduced and voltage drop across the ferroelectric layer (at the same bias) is increased.

In the ferroelectric phase, hysteresis loops of the metal–BST–Si curves are not described in one-dimensional representations, but are determined by changes in external bias which are different for every direction, with the domain system changeover time. Arrangement of the high frequency impedance curve branches along the voltage axis is not symmetrical with respect of the point of origin. This is due to contact potential difference between the field plate and silicon and to the built-in charge concentration in the ferroelectric gap. Therefore, the external voltage drop on one of the branches (left branch in our case, see Fig. 1) will have a higher modulus than the other one. Accordingly, this branch will have a higher reaction to the increment of electronic states localized in the buffer layer as a result of the field stress. This is visualized by a larger shift of the

left loop than that of the right one — thus, the curves also shift towards the positive external voltages and the hysteresis loop widths are reduced.

Heating from room temperature to 121°C brings the BST film in paraelectric state. In this phase, stationary ferroelectric hysteresis loops shall disappear on the curves. The observed loop reverse, see Fig. 3, is indicative of hysteresis effects in the dynamic curves of the measured values as function of the external voltage. Curve shape deviations from the initial curve immediately after cooling down are also indicative of this fact. Temperature 121°C is close to the smeared phase transition region of the BST film from the ferroelectric to paraelectric state. Therefore, fluctuation processes determined by the structure defects and accounting for the phase transition smearing may be regarded as the hysteresis effect sources [12,13].

4. Conclusion

The findings herein show that the patterns of the consequences of field and thermal impacts on the insulating BST film are different. In the first case, this is the generation of additional electronic states localized in the buffer layer at the silicon$-Ba_{1-x}Sr_xTiO_3$ interface. In the second case, this is the manifestation of hysteresis effects as a result of development of the fluctuation processes that account for smearing of the phase transition from the ferroelectric to paraelectric state. Detail study of these phenomena will certainly require different approaches to experimental set up. In the first case, this involves the measurements of electron trap charge localized in the buffer layer. In the second case, there are two methods: measurements of time-impedance dependences after step change in the external voltage and application of different dynamic scanning velocities for bias data recording results.

An important property of metal–ferroelectric–semiconductor thin film structures shall be noted. In the great majority of cases, they use a single silicon wafer for different ferroelectric materials. This means that manifestations of the field impact on these items shall be general in nature and depend to the greater extent on the properties of the buffer layer at the insulator–silicon interface and to a lesser extent on the type of the ferroelectric to be used.

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Conflict of interest

The authors declare that they have no conflict of interest.

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