Distribution of charge carrier concentrations in epitaxial Ge and GeSn layers grown on n^+-Si(001) substrates

© A.M. Titova, S.A. Denisov, V.Yu. Chalkov, N.A. Alyabina, A.V. Zdoroveishchev, V.G. Shengurov

Lobachevsky State University,
603950 Nizhny Novgorod, Russia

E-mail: asya_titova95@mail.ru

Received June 18, 2022
Revised June 25, 2022
Accepted June 25, 2022

Heteroepitaxial Ge or $Ge_{1-x}Sn_x$ layers were grown by hot-wire chemical vapor deposition on Si(001) substrates doped heavily with a donor (As or Sb) impurity. The same layers were also grown on high-resistance Si(001) substrates for comparison. The depth profiles of carrier concentration were measured in both types of layers using the capacitance-voltage method, and carrier mobilities were measured additionally by the Hall effect method in layers on high-resistance silicon. It was found that the layers grown on high-resistance substrates were *p*-type, while the layers grown in the same regimes on heavily doped substrates were *n*-type with electron concentration $n = (4-9) \cdot 10^{16}\,\mathrm{cm}^{-3}$ in Ge layers and $n = (2-4) \cdot 10^{17}\,\mathrm{cm}^{-3}$ in GeSn layers. It was established experimentally and theoretically that the effect of autodoping of Ge and GeSn layers is lacking in the hot-wire chemical vapor deposition method. In our view, the growth of *n*-type Ge and GeSn layers on n^+-Si(001) substrates doped heavily with a donor (As or Sb) impurity is associated with the segregation of this impurity in the process of growth of a buffer Si layer and its subsequent incorporation into growing Ge or GeSn layers.

Keywords: epitaxy, doping, Ge, Si, Sn, concentration.

DOI: 10.21883/SC.2022.09.54124.36

1. Introduction

A number of experimental attempts at integrating photonics with electronics have been made in recent years. Group IV elements (Si and Ge) are the dominant materials of semiconductor electronics. This is attributable to the fact that Ge/Si heterostructures are applicable in the design of a wide variety of semiconductor instruments, such as infrared photodetectors [1], solar cells [2], Ge lasers [3], transistors [4], etc. In addition, Ge/Si heterostructures may be used as epitaxial substrates for the growth of $A^{III}B^{V}$ layers (nitrides included). This should help substitute costly substrates, such as GaAs, Al_2O_3, SiC, etc., with Si ones and provide an opportunity to integrate $A^{III}B^{V}$-based optoelectronic devices with well-developed silicon electronics. However, the fabrication of quality Ge and Si layers is made more difficult by the large mismatch between lattice parameters of Ge and Si (4%) and the difference between thermal expansion coefficients of a Si substrate and a Ge layer ($5.92 \cdot 10^{-6}$ and $2.3 \cdot 10^{-6}\,\mathrm{K}^{-1}$ for Ge and Si, respectively) [5]. This translates into high densities of structural defects in an epitaxial Ge layer, substantial roughness of its surface, and poor electrophysical parameters and hinders the instrumental application of Ge/Si structures.

The usefulness of Si and Ge in optoelectronics is limited by their indirect gap and the associated low efficiency in optoelectronic applications. Layers of $Ge_{1-x}Sn_x$ on Si(001) have become a hot area of research, since this material becomes a direct-gap one at $x = 0.06-0.11$ (depending on the strain) [6,7]. Therefore, recent experiments have been focused on the examination of layers of GeSn solid solutions, which have the potential to be used as direct-gap group IV materials for integration of photonic and optoelectronics within a single chip. A number of experimental studies into the fabrication and characterization of GeSn layers have been published [8–13]. Owing to the large mismatch between lattice parameters of Ge and Sn ($\sim 14\%$), it is difficult to grow layers of solid solution $Ge_{1-x}Sn_x$ with a high percentage of Sn on Si and Ge substrates. In addition, the solubility of Sn in Ge is as low as 0.5%, which makes it difficult to form layers of a solid solution with a high concentration of Sn. Since the surface energy of Sn is lower than the one of Ge, a tendency for surface segregation of Sn in the process of growth is observed.

In spite of these difficulties, considerable efforts were undertaken to grow GeSn layers (primarily by molecular beam epitaxy (MBE) [6,8–12] and chemical vapor deposition (CVD) [8,9,13]). In view of the above, low-temperature growth techniques should be used to grow Ge/Si(001) and GeSn/Si(001) heterostructures. This requirement is also underpinned by the need for *in situ* layer doping. Multilayer epitaxial Ge/Si(001) and GeSn/Si(001) heterostructures, which are used in the design of a number of instruments, contain layers of different conductivity types with different concentrations of the dopant impurity. The method of *in situ* doping of Ge (or GeSn) layers allows one to achieve high electrically active impurity levels in epitaxial layers. It also has an advantage in providing tighter control over the shape of the dopant impurity profile (sharp transitions from an undoped layer to a doped one, and vice versa)

and the positioning of the dopant impurity in a layer. This requirement is crucial for the formation of structures with ultrashallow transitions.

The need to reduce the growth temperature motivated the search for different ways to modify the growth procedure. We chose the hot-wire chemical vapor deposition (HW CVD) technique to grow Ge and GeSn layers on Si(001). It has been used earlier as a low-temperature method for growing epitaxial Si layers [14]. When applied to the growth of germanium on a Si(001) substrate, it yielded layers of only a limited thickness (up to 300 nm) [15].

The low-temperature HW CVD technique differs from common CVD in that the thermal energy needed to decompose precursor gas molecules is provided not by the heating of a substrate to a certain temperature, but by the heating of a hot wire, which is made from Ta or W and in located in the vicinity of a substrate, to a high temperature (1300–2000°C). Precursor fragments (Ge, H, GeH_3, etc.) left after the decomposition of monogermane on a hot wire reach the substrate surface and enable layer growth. We were the first to grow epitaxial Ge layers with a thickness ranging from 0.2 μm to several micrometers and with a sufficiently high degree of structural perfection by HW CVD on Si(001) under a constant low temperature of the Si substrate ($T_S = 350$°C) [16]. We have also developed a technique for MOCVD growth of epitaxial GaAs/Ge/Si(001) substrates, which feature a threading dislocation density in the GaAs layer no higher than $\sim 10^6$ cm^{-2}, based on Ge/Si(001) structures with a thin (0.2 μm) Ge layer [17].

Layers of n^+-Ge with high electron concentrations (up to $1.3 \cdot 10^{20}$ cm^{-3}) were produced via P_2 evaporation from GaP in the process of thermal decomposition of a GaP source by HW CVD [18]. A sublimation source of Ga atoms cut from an ingot of single-crystal germanium doped with gallium was constructed for HW CVD fabrication of *p*-type Ge layers. When the sublimation source was heated (by current passing through it) to a temperature close to the melting point of Ge, mostly Ga atoms evaporated from its surface, since the vapor pressure of this element is ~ 4 orders of magnitude higher than the Ge vapor pressure. Structurally perfect Ge:Ga/Si(001) layers with a hole concentration of 10^{17}–10^{19} cm^{-3} were grown as a result [19]. The fabrication of GeSn/Si(001) layers in our experiments was reported in [20].

The formation of structures with extremely sharp concentration transitions between layers is one of the pressing problems of current epitaxy technology. A high-resistance epitaxial layer on a heavily doped substrate is one of the simplest examples of a structure of this kind. This applies, first and foremost, to the electrically active impurity concentration (i.e., concentration of carriers: electrons and holes), since these parameters are the ones that govern the device operation in most cases.

The aim of the present study was to examine the conductivity type of epitaxial Ge and GeSn layers, which were not doped intentionally; the distribution of concentration of the electrically active impurity (carrier concentration) in them in the process of growth on heavily doped n^+-Si(001) substrates; and the effect of autodoping of an epitaxial germanium layer in the growth chamber of a HW CVD setup.

2. Experimental procedure

Heterostructures (HSs) with Ge or GeSn layers were grown by HW CVD on Si(001) substrates in accordance with a procedure similar to the one detailed in [16,20]. High-resistance KDB-12 Si(001) substrates and substrates doped with antimony (KES-0.01) or arsenic (KEM-0.003) were used for the deposition of Ge and GeSn layers. Following the pre-epitaxial 10-min-long thermal annealing of a substrate at temperature $T_s = 1200$°C, its temperature was reduced to 450–600°C, and a buffer silicon layer was grown by sublimation of a silicon source that was cut from a SI ingot (of the same grade as the substrate). The substrate temperature was then reduced to 300°C (in Ge layer growth) or 200°C (in GeSn layer growth); monogermane (GeH_4) was fed into the chamber, which was filled to $(4–6) \cdot 10^{-4}$ Torr; a Ta wire was heated to 1400°C; and Ge layers were grown. In the process of GeSn layer growth, another step was added to the above procedure: an effusion cell with tin was heated to 900–1040°C [20].

A Ta–Pd–Au Schottky barrier was formed on the surface of layers after metallization and photolithography. The concentration profile and the mobility of carriers were measured using the capacitance-voltage method and the Hall effect method, respectively.

3. Experimental results and discussion

Undoped germanium layers with a thickness of 0.5–2.0 μm deposited by HW CVD onto high-resistance Si(001) substrates had hole conductivity with a hole concentration of $5 \cdot 10^{16}$–$1 \cdot 10^{17}$ cm^{-3}.

Room-temperature Hall measurements demonstrated that Ge layers were *p*-type with a hole mobility of 602 cm^2/V · s (in the layer with the minimum concentration). This conductivity type is associated with the presence of structural defects in Ge layers, which are induced by the mismatch between lattice parameters and produce acceptor states near the valence band edge [3]. A relatively high hole mobility is indicative of a low defect density: the density of etch pits on the layer surface was $N_D \approx 1 \cdot 10^5$ cm^{-2} [16].

Germanium layers of the same thickness grown in the same regimes on Si(001) substrates doped heavily (to $4 \cdot 10^{18}$–$1 \cdot 10^{19}$ cm^{-3}) with donor impurities (As or Sb) were *n*-type with an electron concentration of $(4–9) \cdot 10^{16}$ cm^{-3}.

Figure 1, *a* presents the distribution profiles of the electron concentration in HSs containing epitaxial Ge layers that were deposited in identical regimes onto Si(001) KEM-0.003 substrates within 120 min (curve *1*) and 60 min

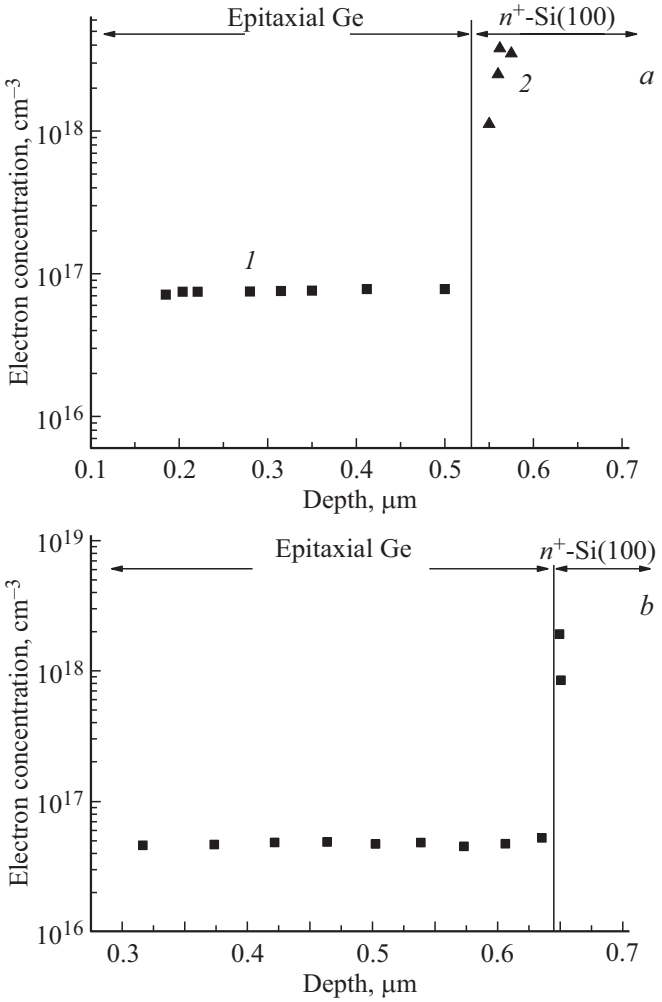

Figure 1. *a* — Distribution of the electron concentration over thickness in epitaxial Ge layers grown on n^+-Si(001) KEM-0.005 substrates with a layer thickness of $1.2\,\mu$m (curve *1*) and $0.6\,\mu$m (curve *2*). *b* — Distribution of the hole concentration in the epitaxial Ge layer with a thickness of $\sim 0.65\,\mu$m grown on a KES-0.01 substrate.

(curve *2*). It can be seen that the electron concentration in the thicker layer (curve *1*) is $\sim (7-8)\cdot 10^{16}\,\mathrm{cm}^{-3}$, while the electron concentration in the thin Ge layer (curve *2*) was measured only at the epitaxial Ge layer / buffer n^+-Si layer interface.

Figure 1, *b* shows the distribution profile of the electron concentration in the Ge layer grown on a KES-0.01 Si substrate. The electron concentration in this Ge layer is somewhat lower than the one presented in Fig. 1, *a* (curve *1*). In view of this, the electron concentration profile was also measured to a greater depth (including the boundary with the n^+-Si-layer).

Layers of GeSn with a thickness of 150–500 nm grown on high-resistance Si(001) substrates were *p*-type. The hole mobility in layers with a thickness of 300 nm and a concentration of $2.1\cdot 10^{18}\,\mathrm{cm}^{-3}$ was $174\,\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$. Note that the hole concentration in $Ge_{1-x}Sn_x$ layers increased from $1.4\cdot 10^{18}$ to $3.5\cdot 10^{18}\,\mathrm{cm}^{-3}$ as the Sn percentage increased from 1 to 3%. The typical distribution profile of the hole concentration in such layers is shown in Fig. 2.

At the same time, GeSn layers grown in the same regimes on substrates doped heavily with a donor impurity were *n*-type. The typical distribution profiles of the electron concentration in such layers are presented in Fig. 3, where curves *1* and *2* correspond to $x = 0.02$ and $x = 0.025$ in $Ge_{1-x}Sn_x$ layers, respectively.

In order to identify the reasons why *n*-type conductivity emerges in Ge and GeSn layers grown on heavily doped substrates, we examined the probability of autodoping of epitaxial layers in our epitaxial growth procedure. The autodoping process is technically possible in HW CVD.

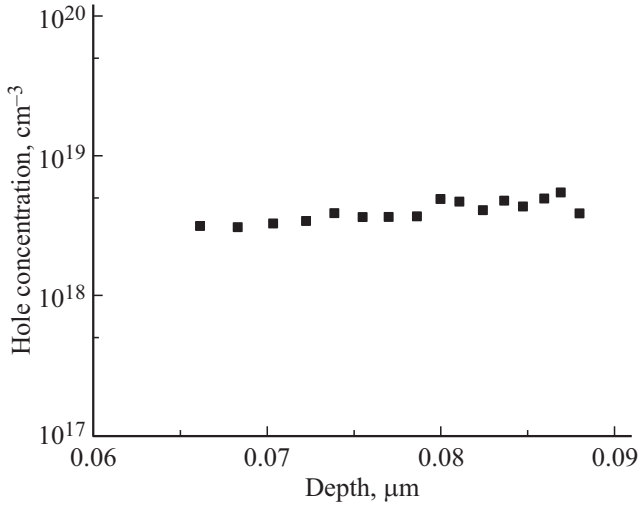

Figure 2. Distribution of the hole concentration over thickness (~ 200 nm) in the epitaxial GeSn layer grown on a high-resistance *p*-Si(001) substrate.

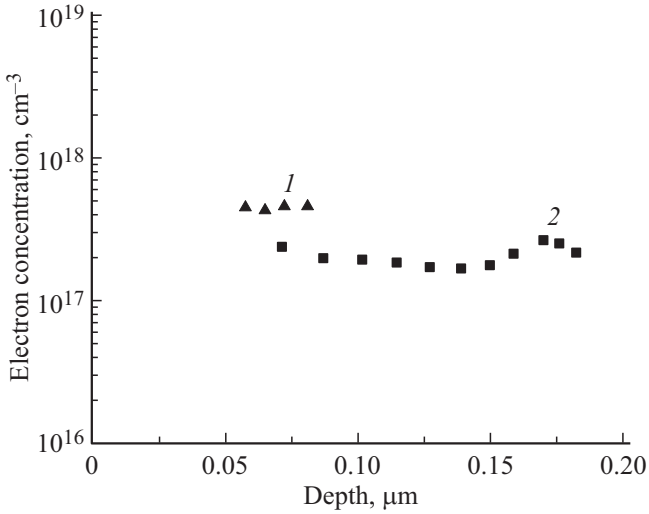

Figure 3. Distribution of the electron concentration over thickness of the epitaxial $Ge_{1-x}Sn_x$ layer grown on a KEM-0.005 n^+-Si(001) substrate. Curve *1* — $x = 2\%$, and the thickness is ~ 160 nm; curve *2* — $x = 2.5\%$, and the thickness is ~ 300 nm.

The impurity evaporating from a heavily doped substrate in the process of its annealing may penetrate into the growing layer following a series of consecutive condensation and re-evaporation events proceeding at structural parts of a growth chamber. The intensity and duration of this „memory“ process are specified by the epitaxial growth conditions. High-resistance silicon layers grown from Si-sublimating sources with an impurity (B) concentration of $\sim 4 \cdot 10^{15}\,\mathrm{cm}^{-3}$ were studied. Layers were deposited at a temperature of $\sim 800^{\circ}\mathrm{C}$ and a rate of $3\,\mu$m/h onto Si(100) substrates doped heavily with arsenic with a concentration of $\sim 1.5 \cdot 10^{19}\,\mathrm{cm}^{-3}$. This deposition was performed using a setup with radiation heating of substrates and a considerable number of structural parts heated to temperatures sufficient for re-evaporation of the mixture. The transition from the annealing regime to the deposition one was implemented by reducing the substrate temperature from $1200^{\circ}\mathrm{C}$ to the layer growth temperature within 3 min. The capacitance-voltage method was applied to examine the distribution of the electrically active impurity concentration in the transition region and compare the obtained results with the theoretical distribution profile of the impurity concentration plotted with the use of Rice nomograms [21]. It was found that these profiles match within the measurement error; therefore, the width of concentration transitions is specified primarily by the diffusion of an impurity from a substrate to a growing layer.

Since the growth of silicon layers in MBE proceeds at relatively low temperatures ($700^{\circ}\mathrm{C}$ and lower), the broadening of the doping impurity profile in the vicinity of the film–substrate transition should not, according to the data derived from Rice nomograms [21], exceed 5 nm. It is assumed here that the coefficient of diffusion of an impurity into an epitaxial layer is the same as the one in a single crystal [22].

Since we performed HW CVD of epitaxial germanium layers onto a Si(001) substrate at a lower temperature ($350^{\circ}\mathrm{C}$), it is fair to assume that the region of impurity diffusion from the heavily doped substrate into the layer should not be larger than 10 atomic layers in size.

However, the coefficient of diffusion in the epitaxial layer was higher in most cases than the common bulk value; therefore, the acceleration in the defect layer needed to be taken into account. Having examined TEM (transmission electron microscopy) images of the cross section of a Ge/Si(001) structure grown by HW CVD, we found regions of strain contrast (associated with mismatch dislocations) near the Ge/Si interface, while the bulk of the epitaxial Ge layer was essentially defect-free [16]. This defect layer was < 200 nm in size. An enhancement of the diffusion coefficient due to structural defects is to be expected in this region [23]. However, Ge layers grown on Si(001) in our experiments were thicker ($\sim 1\,\mu$m) and were doped uniformly with a donor impurity from a heavily doped *n*-type Si substrate throughout their entire thickness.

It is known that donor impurities (antimony and arsenic) are prone to segregation in the process of low-temperature ($\sim 500-600^{\circ}\mathrm{C}$) MBE growth of Si layers [24,25]. In addition, these impurities move from the bulk of a Si substrate to the surface in the process of high-temperature pre-epitaxial annealing, since the vapor pressure of impurity Sb and As at the annealing temperature is several orders of magnitude higher than the one of Si. Impurities (Sb or As) thus rise to the Si substrate surface and are captured by a growing buffer Si layer, which is doped additionally with the same impurity from a sublimation source. The impurity collected at the buffer layer surface starts to penetrate into a Ge or GeSn layer deposited at a low temperature (~ 300 or $200^{\circ}\mathrm{C}$, respectively). Note also that atomic hydrogen, which is a product of pyrolysis of monogermane GeH_4, is involved actively in the HW CVD growth process. It acts as a surface-active agent and facilitates uniform implantation of a donor impurity throughout the thickness of Ge and GeSn layers.

4. Conclusion

It was established experimentally that epitaxial Ge or GeSn layers, which are not doped intentionally, grown at low temperatures by HW CVD on heavily doped Si(001) substrates are *n*-type, while the layers grown in the same regimes on high-resistance Si substrates are *p*-type.

The results of our experiments confirmed that the effect of autodoping of epitaxial Ge and GeSn layers is lacking in the examined growth procedure, since theoretical and experimental distribution profiles of the carrier concentration at the interface between an autoepitaxial high-resistance layer and a heavily doped substrate were matching.

In our view, the growth of *n*-type Ge and GeSn layers on Si(001)substrates, which are doped heavily with a donor impurity and have similar buffer n^{+}-Si layers, is associated with the segregation of this impurity in the process of growth of a buffer Si layer and its subsequent incorporation into growing Ge or GeSn layers.

Funding

This study was supported financially by the Russian Science Foundation (22-22-00866).

Conflict of interest

The authors declare that they have no conflict of interest.

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