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Two-layer logic elements for classic cryogenic computers

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In this paper, for the first time, two-layer logic elements „NOT“, „AND“, „OR“ and „NOR“ were manufactured, in which the heating element of a nanowire in one layer is located in the place where the heated element of another superconductive nanowire is located in a nearest NbN layer. The film thickness of NbN (5−7 nm) was used to form of superconducting nanowires in different layers, and the thickness of Al_2O_3 (25 nm) was used as an interlayer dielectric. The paper shows the design of logic elements, and also demonstrates their operation in pulse mode. The use of multilayer structures without galvanic coupling between nanowires allows the design of multi-level logic devices.

Keywords: NbN thin superconducting films, contactless switching of the superconductor state, cryoelectronic devices, integrated cryogenic resistors, logic elements „NOT“/„AND“/„OR“/„NOR“, cryogenic computers.

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1. Introduction

Over the past few years, National Research Center of „Kurchatov Institute“ has been developing a direction that is dedicated to the design and creation of the main logic elements of classical cryogenic computers. For example, in the work [1] a multistage signal inverter based on nanowires located in one plane and made of superconducting NbN with a thickness of 5−7 nm was created.

The basis of the created logical elements are superconducting nanowires, into which areas of normal metal (resistance) are integrated. Normal metal is obtained from the original superconductor by irradiating it with ion beams of various compositions and energies through masks of the required shape and geometry [2]. The main idea of the functioning of the elements is the forced transfer of a part of the superconducting nanowire to the normal state due to its local heating by a resistor integrated into the adjacent nanowire [3]. This heating is performed without galvanic connection between the gate and the heated section of the nanowire.

Within the framework of the approach used, all nanowires are connected to a constant voltage source, so the appearance of additional resistance in the area of local heating of the nanowire increases its total resistance, the current through it decreases, as a result of which the power released in the normal metal section also decreases, and this nanowire ceases to maintain the normal state in the next nanowire, i.e. the next nanowire will switch to the superconducting state. This principle underlies the design of all basic logic elements.

Previously, we demonstrated a three-stage signal inverter built according to this principle, where all the nanowires were located in one layer [1]. However, the arrangement of nanowires in one plane is not optimal from the point of view of implementing local heating due to the fact that large distances between the gate and the heated section of the nanowire lead to high heat-release rates at the gate.

As we have shown earlier, minimizing the switching power is possible with a two-layer geometry of the gate and the switched nanowire, since the distance between them is determined by the thickness of the interlayer dielectric and can be ~ 10 nm [1].

Earlier, in the 70−80-th years of XX century, cryogenic logic devices were created based on cryotrons [4], which were massive superconductor wires, the switching of which from the superconducting state to the normal state was carried out using a magnetic field created by a superconducting conductor surrounding the switched superconductor. Due to the large size of superconductors, their switching time was $\sim 10^{-4}$ s. Further transition from massive superconductors to thin-film ones made it possible to reduce the switching time to $\sim 10^{-8}$ s [5], and a decrease in the width of the thin-film superconducting element to ~ 100 nm made it possible to reduce the switching time up to $\sim 10^{-12}$ s [6]. In the future, the main direction in the development of superconducting electronics went along the path of forming rapid single flux quantum (RSFQ) logic circuits [7] using Josephson junctions, since the switching energy of a single element in such devices is extremely small. Despite the low switching energy of a single element, the resistive elements that provide the operation of such circuits themselves consumed a lot of power, as a result of which optimized

versions of the power circuits were developed, which were called as eRSFQ. Currently, Hypres [8,9] manufactures eRFQ superconducting logic circuits, which contain several thousand Josephson junctions.

Later, the idea of using superconducting nanosized current gates to create logic elements was presented by a three-terminal device „n-Tron“ [10], in which the transition of the main superconducting nanowire to the normal state was carried out due to overheating narrow area of the gate through which the control signal was applied. Despite the successful fabrication of separate logic elements based on n-Trons, this technology did not on the proper marsh, probably due to the difficulty of taking into account current spreading and arranging their correct balance when designing complex logic circuits. Three-contact elements „Y-Tron“ [11] were also prepared, which use the features of the redistribution of the superconducting current flow density, due to the geometric factor near sharp inhomogeneities of the nanowire side relief, providing optimal conditions for the formation and propagation of a vortex in nanowire. Based on Y-Trons, memory cells [12] were manufactured, but no attempt was made to create logical elements.

In general, it can be noted that all the proposed classical cryogenic circuits based on the control of current devices face the problem of current spreading with a high degree of integration of elements, which limits the possibility of creating units with a large number of elements required for processors.

The most similar in content work using a similar principle of overlapping the superconducting channel due to heating by a gate from a metal gate in the adjacent layer is the work [13]. Heating of a superconducting NbN nanowire (thickness 20 nm) by a metal gate (Ti, thickness 30 nm) located above it through a dielectric layer (SiO_2, thickness 20 nm) was used when creating a two-layer switch element „M-hTron“ by the authors of the work [13], who positioned such an element as promising one for contactless communication of cryogenic circuits with various output loads, including semiconductor devices operating at room temperature. It should be noted that the structure parameters used in [13] (the thickness and width of the NbN superconducting wire, as well as the thickness of the interlayer dielectric) obviously do not meet the requirements for minimizing the power released at the gate to transfer the superconductor to the normal state, since the problem setting was to create an output stage for the implementation of communication of a superconducting circuit with electronics that operates at room temperature. We have previously shown that a decrease in the size of the gate and the switched element leads to the significant decrease in the power required to switch the element, and values of 0.3 nW can be achieved [1]. In order to reduce the switching power, it is necessary to reduce the size of the elements (up to value less than 100 nm) and the thickness of the dielectric, since with a large number of elements this will determine the total energy release in the processor. Simultaneously with a decrease in size (less than 100 nm), the possibility of compaction for the arrangement of elements increases significantly, which is a clear advantage of the proposed approach.

This work did not involve the preparation and demonstration of the creation of logic elements characterized by a minimum switching power, and therefore the sizes of the gates and heated superconductors were made larger than optimal, but at the same time they are less susceptible to external interference in process of operation.

It seems that the proposed approach for the manufacture of full-featured logic elements based on the use of switching without galvanic coupling between the gate and the controlled nanowire will significantly simplify circuit solutions and avoid the problem of spreading and matching currents at a large number of elements under operation. Therefore, our efforts are aimed at demonstrating the possibility of manufacturing basic functional logic elements operating on this principle.

In this work, for the first time, we have prepared demonstration two-layer non-contact logic elements (developed at the National Research Center „Kurchatov Institute“), in which the heating element of nanowire (gate) in one layer is located above/below the heated element of another nanowire in the adjacent layer.

2. Experimental procedure

Superconducting NbN films with thickness of 5−6 nm were deposited on a single-crystal sapphire substrate by cathode sputtering at room temperature of the substrate [14,15]. The Al_2O_3 interlayer dielectric was deposited by the ALD method at temperature of 200°C. The Al_2O_3 thickness was 25 nm.

The preparation of nanostructures was made by electron lithography using a polymethyl methacrylate (PMMA) electron resist on a Helios Nanolab 650 (FEI) scanning electron microscope equipped with a Raith lithographic attachment.

The transformation of superconducting NbN into metal in the required places of nanostructures was carried out by irradiation with a mixed ion beam through windows in protective mask [16,17]. As shown earlier, irradiation of NbN to a fluence of (1−2) dpa (for nitrogen) leads to the formation of the niobium oxynitride phase NbNO [18], which exhibits metallic properties at operating temperature of 4.2 K [16]. The embedding of segments of normal metal into a superconducting nanowire was carried out by irradiating a section of the superconducting nanowire with mixed ion beam to a fluence of $\sim$ 1 dpa through a window in a PMMA mask created by electron lithography. After the preparation of the metal region in the niobium nitride film under the action of irradiation through a mask, the nanowire was formed using a standard electron lithography procedure and subsequent reactive ion etching.

Multilayer structures were created by sequential deposition on the formed first layer containing nanostructures

and measuring contacts of the first layer, layers of the Al_2O_3 interlayer dielectric, and the second layer of niobium nitride. After deposition of the second layer of niobium nitride, measuring contacts of the second layer were created on it and electron lithography was carried out to form the required configuration of nanowires and integrated resistances. If it was necessary to create resistances in the nanowires of the second layer, ion irradiation of sections of the second layer was carried out to the fluence ~ 1 dpa through a window in the PMMA mask created by electron lithography.

After preparation, the multilayer samples were single annealed in vacuum at temperature of 200°C for 1 hour to stabilize the electrophysical characteristics of the irradiated areas, and partially annealed for radiation defects in the irradiated zone.

The measurement of electrophysical characteristics and demonstration of the operation of logic elements were carried out using the Keithley-4200 measuring system, which is designed to test circuits in low-frequency modes. To demonstrate the correct operation of the devices, the input signals were applied by means of this measuring system in quasi-stationary mode, which was the reason for the large values of the pulse duration. To reduce the influence of external interference on the operation of logic devices, their input and output stages were equipped with passive filters that did not allow a significant increase in the frequency of pulses to the devices.

Demonstration of the operation of devices at high frequencies will continue in the future, together with the development of signal filtering circuits that allow such measurements to be made.

3. Results and discussion

In this work, various types of two-layer logic elements were made: „NOT“, „NOR“, „AND“ and „OR“.

Figure 1, *a* shows the diagram of two-layer logic element „NOT“, and Figure 1, *b* shows the raster image of the created element in secondary electrons. The gate contains the resistance R_g (contacts *1–6*) as well as the output stage (contacts *3–4*) in the lower layer. The upper layer contains a nanowire (contacts *2–5*) connected to the constant voltage source, in which the integrated resistance R is formed. The principle of operation of the element is as follows. In the absence of a signal at the gate R_g, the current flowing through the upper nanowire is maximum, the resistance R heats up the section of the output nanowire (contacts *3–4*), and there is a high signal level at the output. As soon as a signal is applied to the gate, the built-in resistance R_g heats up the sections of the superconductor above it in the upper layer, the resistance of the nanowire (contacts *2–5*) in the upper layer increases, the current through it drops, and the built-in resistance R stops heating the output stage (contacts *3–4*), as a result of which the output signal goes to zero. Figure 1, *c* shows an oscilloscope record of the operation of the logic element „NOT“ in the pulsed mode. As can be seen from Fig. 1, *c*, the logic element operates in accordance with the required truth table: in the absence of a signal at the input, a high signal is observed at the output; when a high signal is applied to the input, the output signal drops to zero.

The circuit for measuring the electrical characteristics of the logic element „NOT“ is shown in Fig. 1, *d*. Contact *2* is connected to a DC voltage source. Input signal is applied to the contact *1*. As an output stage, a superconducting nanowire (*3–4*) is used, connected to a direct current source, the value of which is chosen less than the critical current value for this nanowire.

Figure 2, *a* shows a diagram of a two-layer logical element „NOR“, and Figure 2, *b* shows the raster image of the created element in secondary electrons. Two gates R_1 (contacts *1–5*) and R_2 (contacts *3–5*), as well as an output stage (contacts *2–5*) are located in the lower layer. The upper layer contains a nanowire (contacts *6–4*) connected to the constant voltage source, in which an integrated resistance R is formed. The principle of operation of the element is as follows. In the absence of a signal at the R_1 and R_2 gates, the current flowing through the upper nanowire is maximum, the resistance R heats up the section of the output nanowire (contacts *2–5*), and there is a high signal level at the output. As soon as a signal is applied to one or both gates, the built-in resistances R_1 and/or R_2 heat up the sections of the superconductor above them in the upper layer, the resistance of the conductor (contacts *6–4*) in the upper layer increases, the current through it drops, and the built-in resistance R stops heating the output stage (contacts *2–5*), as a result of which the output signal goes to zero. Figure 2, *c* shows an oscilloscope record of the operation of the logic element „NOR“ in the pulsed mode. As can be seen from Fig. 2, *c*, the logic element operates in accordance with the required truth table: in the absence of a signal at both inputs, a high signal is observed at the output, when a high signal is applied to one or both inputs, the output signal drops to zero.

The circuit for measuring the electrical characteristics of the logic element „NOR“ is shown in Fig. 2, *d*. The input signals are applied to the contacts *1* and *3*, respectively. Contact *6* is connected to a DC voltage source. As an output stage, a superconducting nanowire (*2–5*) is used, connected to a direct current source, the value of which is chosen less than the critical current value for this nanowire.

Figure 3, *a* shows a diagram of a two-layer logical element „OR“, and Figure 3, *b* shows the raster image of the created element in secondary electrons. Two gates R_1 (contacts *1–6*) and R_2 (contacts *3–4*) are located in the lower layer. The upper layer contains the output nanowire (contacts *2–5*) divided into two superconducting channels located above the gate resistances in the lower layer, which is connected to direct current source. The principle of operation of the element is as follows. In the absence of a signal at the R_1 and R_2 gates, the upper nanowire is in the superconducting state, and the output voltage is equal to

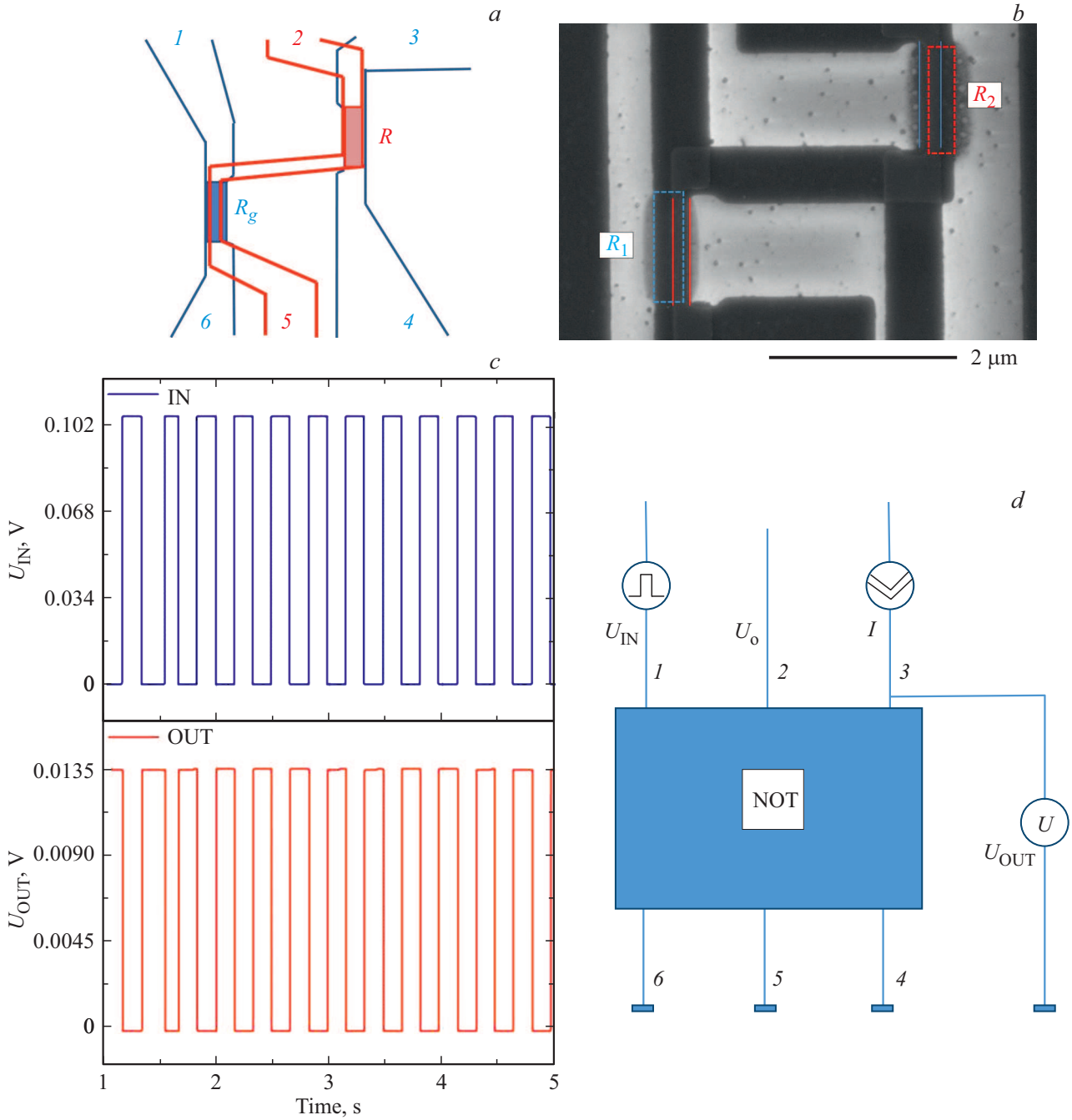

Figure 1. Two-layer logical element „NOT “. *a*) Principal diagram: *1*–*6* is R_g gate (bottom layer), *2*–*5* is R (upper layer), *3*–*4* is output (lower layer). *b*) SEM image of an element in secondary electrons. *c*) Oscilloscope records of element operation. Input (IN) — contacts *1*–*6*, output (OUT) — contacts *3*–*4*. *d*) Scheme of electrical measurements of the element „NOT“: contact *1* — input signal; contact *2* — reference voltage U_o; contact *3* — constant current source I; contacts *4*–*6* — ground.

zero. When a signal is applied to only one of the gates, this gate starts to heat up the superconductor above it, and it goes into the normal state. The current flowing through the upper bifurcated nanowire (*2*–*5*) is selected so that it is less than twice the critical current of one narrow section of the superconducting nanowire. Therefore, the transition of only one of the narrow sections of the nanowire to the normal state does not cause the same transition of the second narrow section. Complete overlap of the superconducting channel (2–5) takes place only when the input signal is simultaneously applied to both gates. In the latter case, a high signal level occurs at the output (*2*–*5*). Figure 3, *c* shows an oscilloscope record of the operation of the logic element „OR“ in the pulsed mode. As can be seen from Fig. 3, *c*, the logic element operates in accordance with the required truth table: if there is no signal at both inputs or if

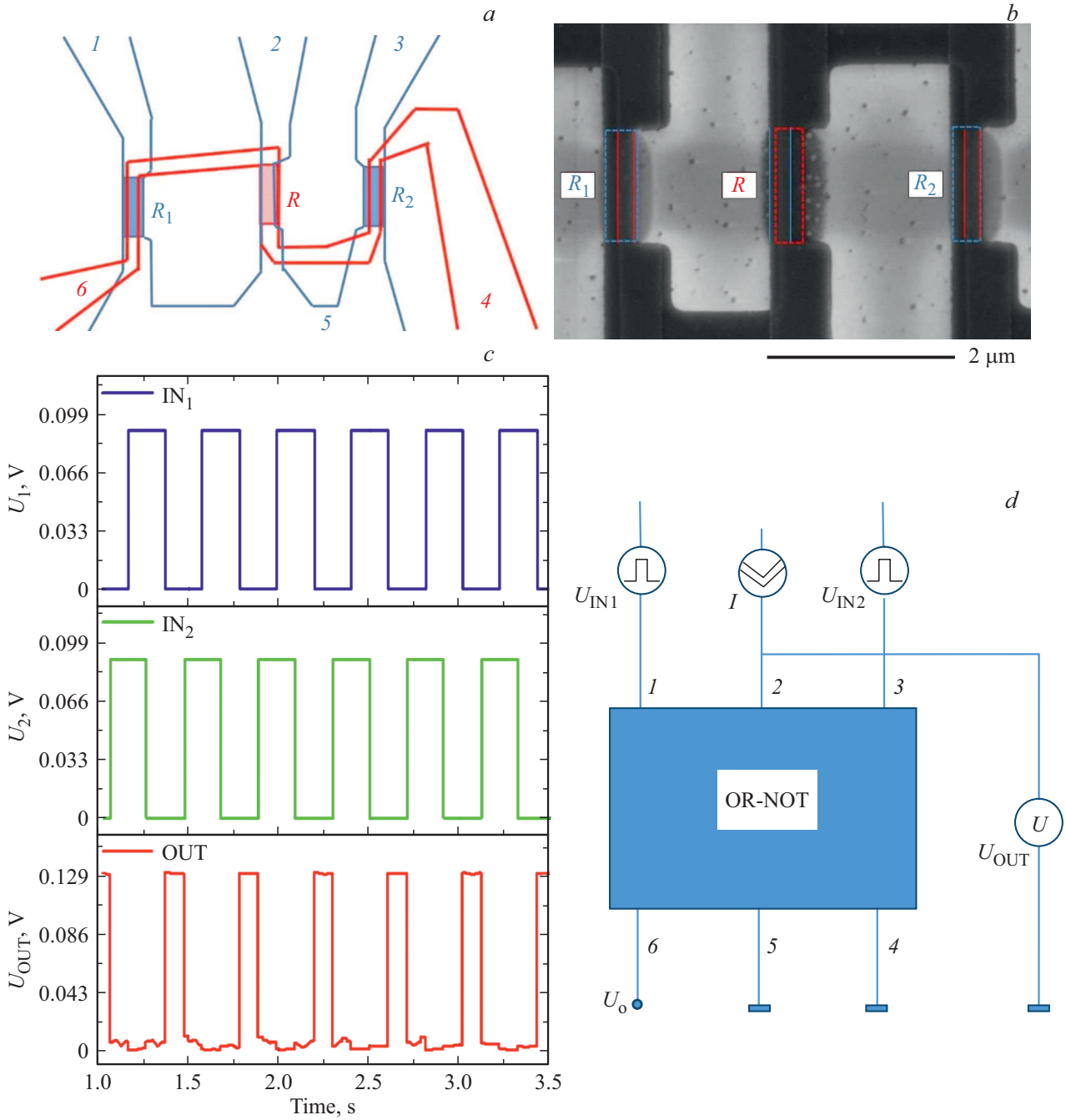

Figure 2. Two-layer logical element „NOR“. *a*) Principle diagram: first input R_1 (*1*–*5*) and second input R_2 (*3*–*5*) (lower layer), nanowire with resistance R (*6*–*4*) (upper layer), output (*2*–*5*) (lower layer). *b*) SEM image of an element in secondary electrons. *c*) oscilloscope records of element operation. Input 1 (IN_1) (contacts *1*–*5*), input *2* (IN_2) (contacts it3–5), output (OUT) (contacts *2*–*5*). *d*) Scheme of electrical measurements of element „NOR“: contact *1* — input signal 1; contact *2* — constant current source *I*; contact *3* — input signal — 2; contacts *4* and *5* — ground; contact *6* — reference voltage U_0.

there is a signal at only one input, a low signal is observed at the output. High signal at the output is observed only when a high signal is applied to both inputs at the same time.

The circuit for measuring the electrical characteristics of the logic element „AND“ is shown in Fig. 3, *d*. The input signals are applied to the contacts *1* and *3*, respectively. As an output stage, a bifurcated (consists of two parallel segments) superconducting nanowire (*2*–*4*) is used, connected to a direct current source, the value of which is chosen less than the critical current value of one of the narrow segments. The last requirement ensures complete overlapping of the superconducting channel only when a signal is simultaneously present at both inputs.

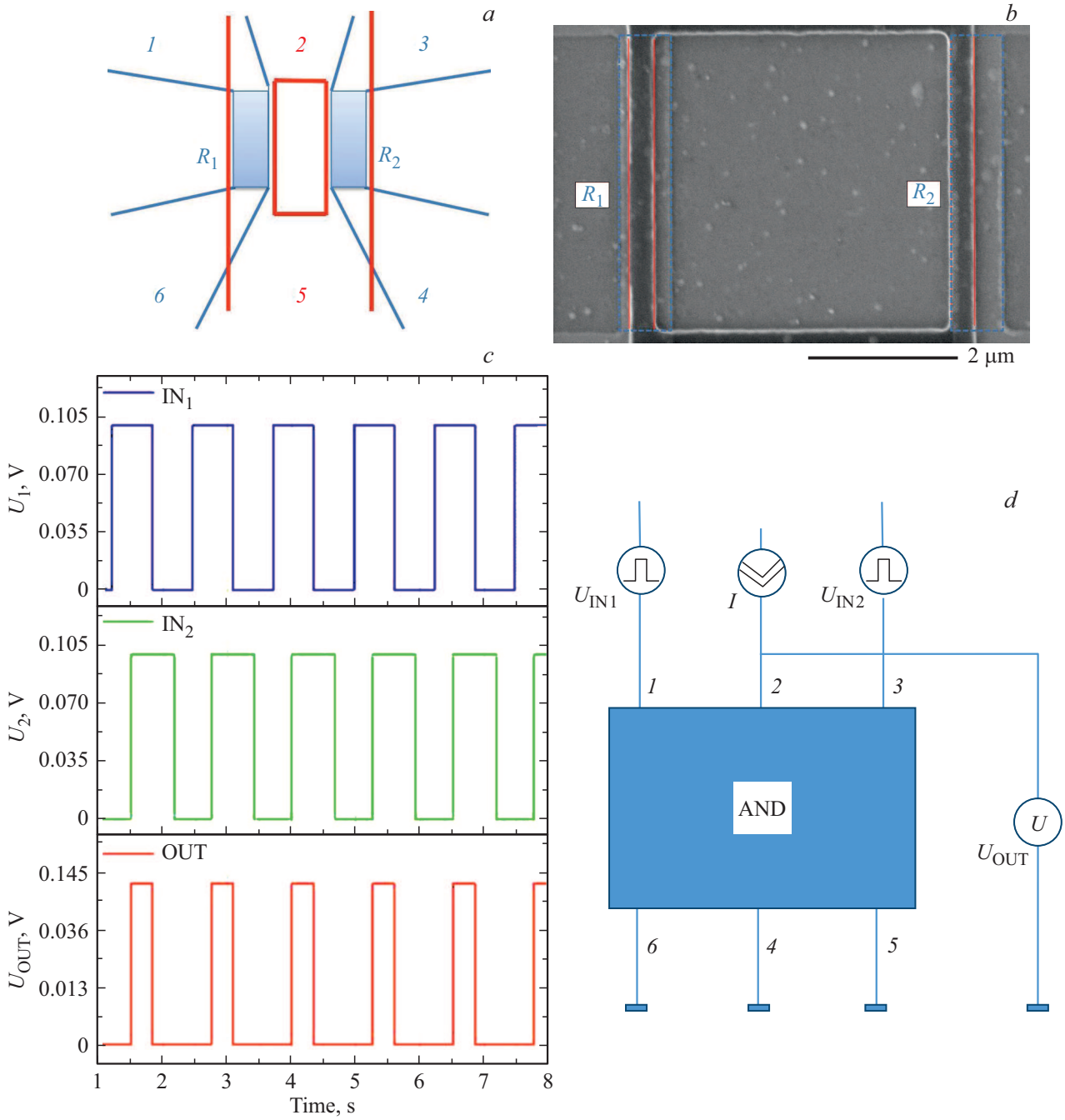

Figure 3. Two-layer logical element „ AND“. *a*) principle diagram: first input R_1 (*1*–*6*) and second input R_2 (*3*–*4*) (lower layer), output (*2*–*5*) (upper layer). *b*) SEM image of element in secondary electrons. *c*) Oscilloscope records of element operation. Input *1* ($IN_{1)}$ (contacts *1*–*6*), input *2* (IN_2) (contacts *3*–*4*), output (OUT) (contacts *2*–*5*). *d*) Scheme of electrical measurements for the element „AND“: contact *1* — input signal № 1; contact *2* — constant current source *I*; contact *3* — input signal № 2; contacts *4*–*6* — ground.

Figure 4, *a* shows the diagram of two-layer logic element „OR“, and Figure 4, *b* shows the raster image of the created element in secondary electrons. Two gates R_1 (contacts *1*–*6*) and R_2 (contacts *3*–*4*) are located in the lower layer. The upper layer contains a nanowire (contacts *2*–*5*) connected to a direct current source. The principle of operation of the element is as follows. In the absence of a signal at the R_1 and R_2 gates, the upper nanowire is in the superconducting state, and the output voltage (*2*–*5*) is equal to zero. When a signal is applied to one of the gates or both at once, the resistance of the gate (gates) begins to heat up sections of the superconducting nanowire (*2*–*5*) of the upper layer, as a result of which a voltage appears at the output (*2*–*5*). Figure 4, *c* shows an oscilloscope record of the operation of the logic element „OR“ in the pulsed mode. As can be seen from Fig. 4, *c*,

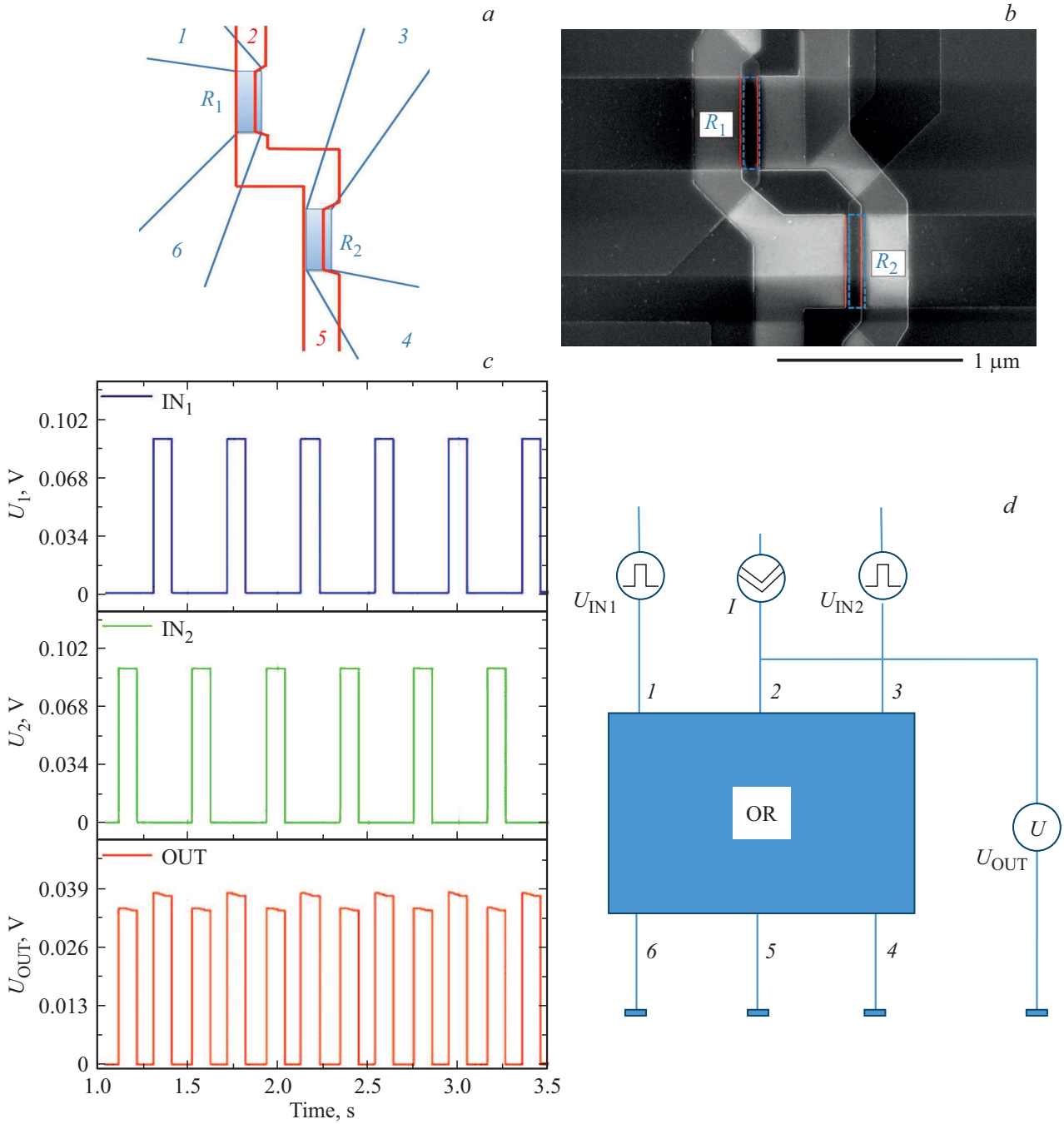

Figure 4. Two-layer logical element „OR“. *a*) Principal diagram: first input R_1 (*1*–*6*) and second input R_2 (*3*–*4*) (lower layer), output (*2*–*5*) (upper layer). *b*) SEM image of an element in secondary electrons. *c*) Oscilloscope records of element operation. Input *1* (IN_1) (contacts *1*–*6*), input *2* (IN_2) (contacts *3*–*4*), output (OUT) (contacts *2*–*5*). *d*) Scheme of electrical measurements of element „OR“: contact *1* — input signal № 1; contact *2* — constant current source *I*; contact *3* — input signal № 2; contacts *4*–*6* — ground.

the logic element operates in accordance with the required truth table: if there is no signal at both inputs, a low signal is observed at the output, when a high signal is applied to one or both inputs, high signal appears at the output.

The circuit for measuring the electrical characteristics of the logic element „OR“ is shown in Fig. 4, *d*. The input signals are applied to the contacts *1* and *3*, respectively. As an output stage, a superconducting nanowire (*2*–*5*) is used, connected to a direct current source, the value of which is chosen less than the critical current value for this nanowire.

The creation of multilayer structures can significantly increase the element density in a cryogenic processor.

The further development prospect of the work is associated with a decrease in the size of the switched elements and gates, a decrease in the thickness of the interlayer dielectric; conducting experiments to measure the operation

of devices at high frequencies; creating more complex functional devices based on single logical elements and demonstrating their correct operation. It seems that under these conditions, it is possible to reduce the switching power to a level of several tens of pW, which will make it possible to manufacture devices with an average degree of integration that consume power acceptable for such circuits even taking into account the additional power consumed to maintain the cryogenic temperature of the device, which will make them competitive compared to modern semiconductor analogous solutions both in terms of power consumption and maximum operating frequencies.

Since the non-contact heating method used for switching elements includes a sequence of physical processes of heat transfer from the heater to the superconductor through the interlayer dielectric, it is not possible to formulate simple equations relating the critical material parameters of structures to the frequency characteristics of devices based on them. Apparently, it is advisable to perform numerical estimates that describe the propagation of heat from the heater to the heated section of the superconducting nanowire based on the fundamental equations of heat conduction, taking into account the sequential interaction of the electronic and phonon subsystems of the heater, separating dielectric and superconductor, as it is done in detail in the work [13]. In the work [13], the equations of thermal conductivity describing the sequential propagation of heat from the electrons of the heater to the phonons of the heated superconductor, as well as the physical constants necessary for such calculations, are presented.

The simulation data obtained in the work [13] indicate that the problem of achieving short switching times requires reducing the size of elements both for the parameters of the structures made in the work [13] and for structures used in the current work. Reducing the size of the elements will also lead to a decrease in the power consumption of devices [19], which makes this approach attractive given the well-known problems of modern semiconductor circuits.

The objectives of this work did not include the simulation of the time parameters of heat propagation during a single switching, which would allow us to estimate the limiting frequencies for the operation of devices, since a separate publication is planned on this topic, together with measurements of the operation of devices at high frequencies. The planned high-frequency measurements will require a different technique for conducting electrical measurements, including the organizing of dispersionless microwave waveguides, as well as the development of a special topology of the arrangement of elements to minimize crosstalk.

4. Conclusion

In work, for the first time, a complete set of necessary basic logic elements for a classical cryogenic computer („NOT“, „NOR“, „AND“, „OR„) has been created. The elements are prepared in a two-layer geometry, which allows minimizing the distance between the heater and the heated section of the superconducting nanowire, thereby reducing their power consumption. The multilayer arrangement of logic elements and the absence of galvanic coupling between individual elements make it possible to simplify the circuitry of devices and significantly increase the density of elements in a cryogenic processor.

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Conflict of interest

The authors declare that they have no conflict of interest.

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