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Influence of a multilayer grounded field plate on the effect of quasi-saturation of current-voltage chatacteristics of power radio frequence lateral transistors

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Was been performed modeling of LDMOS-transistor structures with two- and three-layer grounded field plates. On both structures the manifestation of the effect of quasi-saturation of $I_D - V_D$ characteristics was estimated. It is shown that the new design of the three-layer grounded field plate significantly suppresses the effect of quasi-saturation.

Keywords: power RF transistors, LDMOS, quasi-saturation of $I-V$ characteristics.

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1. Introduction

LDMOS (Laterally Diffused Metal Oxide Semiconductors) transistors are the most advanced silicon-based devices among discrete high-power ultrahigh frequency (UHF) transistors [1]. Their scope includes: base stations of a cellular communication system, radio transmitters of P-, L-, S-bands of frequency, TV signal transmitters of DVB-T/DVB-T2 standards, radar ground and airborne stations, navigation systems etc. Despite the predicted displacement of LDMOS technology by devices based on new semiconductor materials, in particular gallium nitride, these technologies continue to coexist and compete. The advantages of LDMOS transistors are lower cost with rather high energy parameters [2] and mature production technology. Foreign manufacturers of UHF transistors not only retain the traditionally strong positions of LDMOS technology in the niche of devices with operating frequencies up to 2 GHz, but also plan to expand the scope of LDMOS transistors to frequencies 12 GHz [3], which are often associated with devices based on gallium nitride. It is noteworthy that same manufacturers also have a line of devices based on gallium nitride [4].

Quasi-saturation of current-voltage curve (CVC) is a negative effect that occurs during the current flow in LDMOS transistor. The quasi-saturation occurrence is a consequence of the Kirk Effect [5]. Briefly, the Kirk effect can be described as follows. As the gate voltage U_g increases at a fixed drain voltage U_d, more and more electrons are injected from the channel region into the relatively lightly doped drain region (hereinafter, the LDD region). At a certain U_g the n carriers density will exceed the dopant concentration in the LDD region N_{LDD}. This will lead to electric field strength E decreasing in the LDD region near the gate edge and E increasing at the LDD/n^+-drain boundary. The field increasing at drain boundary causes saturation of the electron velocity.

Another, equally important, cause of saturation is the screening of the drain field, which accompanies the Kirk effect. As n grows, the total field of injected carriers begins to screen the channel region from the drain voltage. Thus, the gate voltage increasing reduces the pulling field of the drain, which eventually causes the transient CVC saturation, even if the carriers speed is far from saturation. Together, the Kirk effect and drain screening cause quasi-saturation of the CVC [6,7].

Strongly pronounced quasi-saturation results in a number of problems that can deteriorate the parameters of UHF transistors and devices based on them. It is shown that the quasi-saturation effect decreasing has a positive effect on the reliability of UHF transistors [8] and on the resistance of the transistor to breakdown through a parasitic bipolar transistor [9].

In the article [10] it was stated that the most effective way to reduce the degree of quasi-saturation is to improve the grounded field plate (GFP). Currently, the domestic industry is improving the manufacturing technology of LDMOS transistor crystals, which is expected to result in the introduction of a three-layer GFP. This article relates to the consideration of the consequences of three-layer GFP introduction from the point of view of the quasi-saturation effect suppression.

2. Experiment procedure

To identify the effect of a three-layer GFP on the degree of intensity of quasi-saturation of the output CVC a model of high-power UHF LDMOS transistor was built in the instrument-technological design environment Sentaurus TCAD. This model is based on the actual technology

of manufacturing the transistor crystals of this type and includes the simulation of all main technological operations for creating LDMOS structure from epitaxial growth to deposition passivation.

To create this model, the following software modules from the Sentaurus TCAD package were used:

– Sentaurus Process (SProcess) — for modeling LDMOS transistor structure;

– Sentaurus Device (SDevice) — for calculating the electrophysical processes occurring in the LDMOS-structure model and plotting CVC;

– Inspect — to calculate the electrical parameters that act as criteria for the degree of quasi-saturation.

The criterion for the degree of quasi-saturation is the parameter ΔI_d, called the relative increment of the drain current and calculated by the formula

$$\Delta I_d = \frac{I_d(U_d = 40\,\text{V}) - I_d(U_d = 20\,\text{V})}{I_d(U_d = 20\,\text{V})},$$

where I_d — drain current.

This criterion makes it possible to estimate the CVC deviation from ideal saturation (complete absence of drain current dependence on the drain voltage). For a transistor with ideal saturation, $\Delta I_d = 0$ and, accordingly, the larger the value of ΔI_d is, the more pronounced the quasi-saturation is. The choice of the $U_d = 20$ V point is due to the fact that at this voltage, CVC of the transistor, without taking into account the effect of quasi-saturation, reliably reach the ideal saturation. The point $U_d = 40$ V was chosen for reasons of convenience. Normalization to the value of the drain current makes it possible to compare the increments of the drain current at different levels of the drain current and, accordingly, U_g.

3. Experimental results

Based on the developed model, three options of the LDMOS transistor structure were considered. The first option is a classic LDMOS transistor design, including a simple single-layer GFP made in the first layer of current-carrying metal (Fig. 1, *a*). The second option is a more advanced design, in which GFP layer is added, located near the surface of the silicon substrate and made in a thin layer of refractory metal (Fig. 1, *b*). Finally, the third option — the construction of three-layer GFP currently being developed (Fig. 1, *c*).

GFPs of different designs are characterized by different field effect on the area of LDD region located under them. This leads to the fact that in each design the optimal impurity concentration in the LDD region, i.e., the concentration at which the maximum possible drain-source breakdown voltage level is observed, differs. For classical GFP it is $6.0 \cdot 10^{16}\,\text{cm}^{-3}$, for two-layer GFP — $7.6 \cdot 10^{16}\,\text{cm}^{-3}$, for three-layer GFP — $8.3 \cdot 10^{16}\,\text{cm}^{-3}$ (hereinafter, the concentration at the peak of the distribution

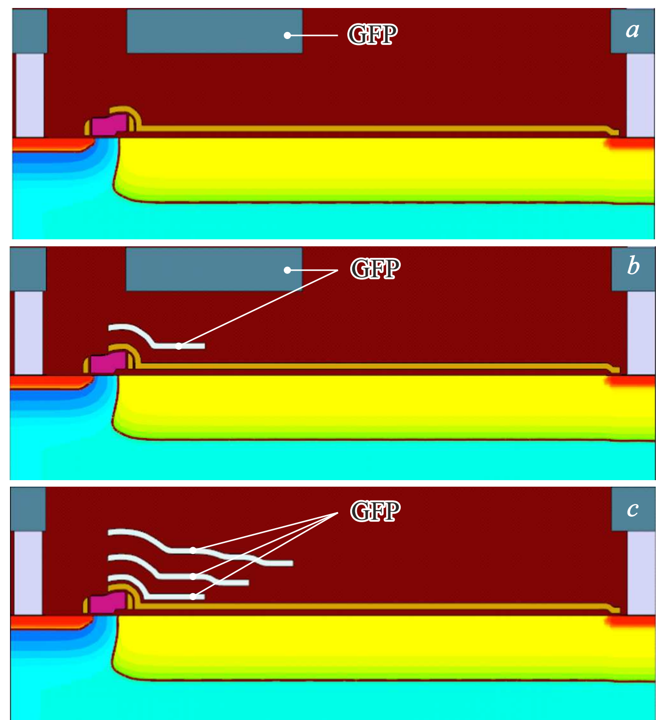

Figure 1. Sentaurus TCAD model of LDMOS structure with classical GFP (*a*); two-layer GFP (*b*); three-layer GFP (*c*).

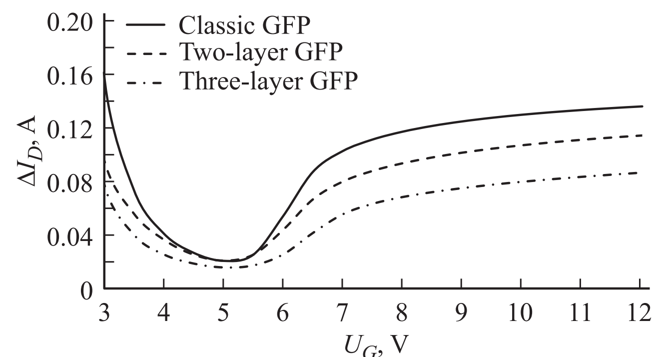

Figure 2. Comparison of the relative increments of the drain current of LDMOS structures of different designs at optimal N_{LDD}.

is implied; for all designs the doping energy and the drive-in mode are identical). The drain-source breakdown voltage at the optimum concentration in these cases is 116, 123 and 124 V, respectively.

For all options, families of output CVCs were plotted at gate voltages (3–12) V, and the relative increments of the drain current ΔI_d were calculated. When comparing ΔI_d values, it is worth bearing in mind that N_{LDD} value itself affects the degree of quasi-saturation. In view of the above, the comparison of the structures under study by the level of ΔI_d was given both at N_{LDD}, corresponding to the optimal concentration for each structure (Fig. 2), and at the same N_{LDD} — $6.0 \cdot 10^{16}\,\text{cm}^{-3}$ (Fig. 3).

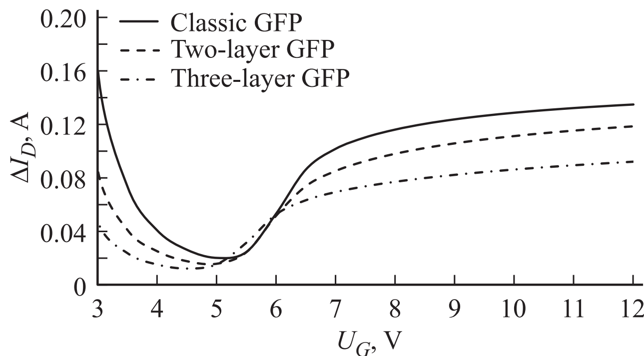

Figure 3. Comparison of the relative increments of the drain current of LDMOS structures of different designs at $N_{\text{LDD}} = 6.0 \cdot 10^{16}\,\text{cm}^{-3}$.

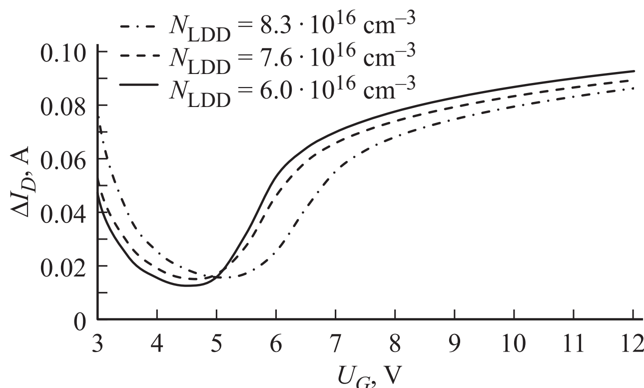

Figure 4. Comparison of the relative increments of the drain current of LDMOS structures with three-layer GFP at different N_{LDD}.

To estimate the influence of N_{LDD} on the degree of quasi-saturation, Fig. 4 shows the dependences ΔI_d on the gate voltage for a design with three-level GFP.

4. Results and discussion

Based on the data obtained (Fig. 2), the introduction of three-layer GFP into the design of LDMOS transistor compared to design with two-layer GFP makes it possible to reduce the relative increment of the drain current depending on the level U_g by (20−60)% (average decreasing — 38%). This indicates a significant decrease in the degree of quasi-saturation.

At the same time, comparing the data in Fig. 2 and 3, we can conclude that the main role in the decrease in ΔI_d was played by the introduction of three-layer GFP, but not the accompanying increase in the impurity concentration in the LDD region, although in the previous study the opposite was considered [10]. This discrepancy is due to the fact that in the earlier study only the classical option of GFP was considered, which has a relatively weak field effect on the LDD region. Also, the conclusion about the relatively weak effect of N_{LDD} on quasi-saturations is confirmed by the data of Fig. 4 — in the range U_g from the threshold voltage to the voltage corresponding to the minimum ΔI_d (hereinafter $U_{g\,qs\,\min}$), increase in N_{LDD} even leads to increase in ΔI_d. In general, when plots are superimposed by $U_{g\,qs\,\min}$ points, the change in N_{LDD} from $6.0 \cdot 10^{16}$ to $8.3 \cdot 10^{16}\,\text{cm}^{-3}$ (which corresponds to the doping dose increasing by 40%) leads to ΔI_d drop by (10−20)% only.

The shift of the $U_{g\,qs\,\min}$ point with N_{LDD} increasing is explained by the shift in the gate voltage level, at which the Kirk effect occurs. $U_{g\,qs\,\min}$ corresponds to the situation when the Kirk effect already started to occur, but was not yet passed into its terminal stage, and the field strength E is distributed relatively uniformly along the LDD region [7]. In turn, N_{LDD} determines at what level of electron injection from the channel (and correspondingly U_g) the Kirk effect begins to occur, since the necessary initial condition for its occurrence is the excess the concentration of injected electrons over the impurity concentration in the LDD region.

The explanation why the introduction of three-layer GFP contributes to degree of quasi-saturation decreasing is the stronger field action of the three-layer GFP, which causes E redistribution along the LDD region. At voltages $U_g = U_{g\,qs\,\min}$ and lower (Fig. 5) GFP suppresses a sharp peak of strength at the gate edge and forms additional peaks corresponding to the edges of GFP. Due to this, the area of the LDD region, where the electron speed reaches saturation, increases, which contributes to the drain current increment decreasing. At voltages above $U_{g\,qs\,\min}$ (Fig. 6), the GFP weakens the Kirk effect, preventing the field strength decreasing at the gate edge. The described effects are valid for the GFP of all the structures under consideration, however, due to the greater field effect in the structure with three-layer GFP, they are more pronounced. This is clearly seen in Figs 5 6: the E peaks corresponding to the GFP edges are always higher in the case of three-layer GFP than in the case of two-layer one.

From Fig. 6, one may get the impression that the field distribution in the case of two-layer GFP is more uniform and, therefore, should correspond to a smaller ΔI_d. However, such distribution leads to the fact that the drift speed of electrons does not reach full saturation. In the

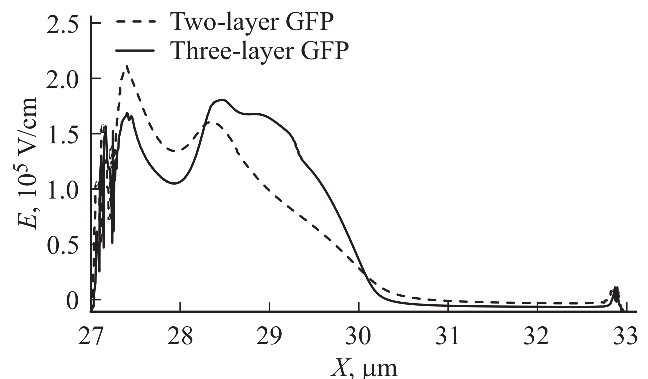

Figure 5. Distribution of E along the LDD region; $U_G = 4\,\text{V}$, $U_C = 40\,\text{V}$.

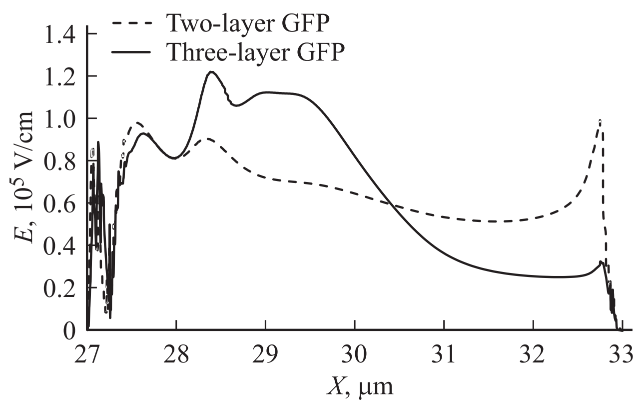

Figure 6. Distribution of E along the LDD region; $U_G = 6$ V, $U_C = 40$ V.

first approximation, it can be assumed that the complete saturation of the drift speed starts from $E = 10^5$ V/cm. It can be seen in Fig. 6 that the field strength along almost the entire length of the LDD region in the case of two-layer GFP is lower than 10^5 V/cm.

5. Conclusion

The simulation performed showed that:

– the use of the LDMOS-structure design with three-layer GFP makes it possible to significantly reduce the degree of quasi-saturation in comparison with the existing design;

– the decrease in the degree of quasi-saturation is due to a stronger field effect and increase in the impurity concentration in the LDD region, at that the first factor being the determining one.

Thus, the introduction of three-layer GFP into the design of LDMOS transistor crystal has a positive effect on the quasi-saturation effect suppression.

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Conflict of interest

The authors declare that they have no conflict of interest.

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