Studying $C-V$ characteristics of MIS structures with ALD Al_2O_3 on n- and p-CdHgTe stabilized with ultra-thin native oxide

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Capacitance–voltage characteristics of metal dielectric semiconductor structures with atomic layer deposition Al_2O_3 on n- and p-$Cd_{0.22}Hg_{0.78}Te$ (with and without a surface graded-gap layer) preliminary oxidized in oxygen glow discharge plasma (with the resulting oxide thickness of 2 nm) have been studied. The obtained structures reveal the positive fixed charge with a density of $\sim (1-6)\cdot 10^{11}$ cm^{-2}. The ratio between a slow surface states density and a surface band gap width is almost independent on graded-gap layer presence, with the value of $\sim (4-8)\cdot 10^{11}$ cm$^{-2}\cdot$ eV^{-1}. The proposed passivation approach provides near-ideal low-frequency capacitance-voltages characterized by weak influence of fast surface states. Films of CdHgTe grown without the graded-gap surface layer are proved to be much more sensitive to the process of oxidation in glow discharge plasma.

Keywords: mercury cadmium telluride, film, surface states, plasma.

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1. Introduction

One of the key technological goals in fabrication of infrared photodetectors based on narrow-gap semiconductor compounds consists in maintaining a high quality of the semiconductor surface and interfaces. With a band gap being as small 0.1−0.4 eV, even relatively low densities of the fixed charge of an insulator and surface states at the insulator−semiconductor interface may alter significantly the surface potential and induce the emergence of a „parasitic“ spatial charge region or even a surface conductance channel [1,2]. Leakage and dark currents of a photodetector increase as a result, and this has a negative effect on its characteristics (e.g., sensitivity, detectivity, and noise level [3]).

Mercury cadmium telluride (MCT, CdHgTe), which is used to fabricate focal plane arrays (FPAs) with an absorption edge through to the far IR range and is potentially applicable in the terahertz range, is highly sensitive to external physical, chemical, and thermal impacts. If the MCT surface structure is damaged and its chemical composition is altered in certain technological operations in the course of device fabrication, electrically active defects, which have a negative effect on the characteristics of the devices being produced, emerge. In view of this, strict requirements regarding the minimization of negative impact on the semiconductor as a whole and its surface in particular are imposed on all fabrication processes.

The MCT surface is commonly passivated with an insulator or a wide-gap semiconductor via physical or chemical vapor deposition [4–9]. However, such methods, first, often involve substrate heating in vacuum and, second, may lead to physical mixing and chemical interaction between the deposited material and MCT. The research into refinement of the existing CdHgTe passivation techniques and development and characterization of new ones still remains topical [10–17].

We have proposed to use an ultrathin (< 5 nm) native oxide (NO) to stabilize the CdHgTe surface. This oxide should form a quality interface with the semiconductor and protect it from the negative influence of subsequent technological processes (deposition of a protective insulator and (or) antireflective coating, metallization, etc.). A similar approach has been demonstrated, e.g., in [18–20], where the excitation of oxygen atoms by UV irradiation or high-frequency oxygen plasma were used to oxidize MCT. The data presented in these papers suggest that a native MCT oxide interlayer with a thickness of 30−40 nm provides an opportunity to reduce considerably the densities of the fixed charge and slow surface states, although the density of fast surface states remains at the level of $\sim 1\cdot 10^{11}$ cm$^{-2}\cdot$ eV^{-1}. Our approach is fundamentally different in that the NO layer is ultrathin (i.e., has a thickness of just several nanometers). Since the oxidation process in itself is known to induce changes in the chemical composition of the near-surface MCT region with a thickness up to several tens of nanometers [21,22], it is expected that a reduction in the oxide thickness should help minimize the negative effect on the semiconductor interface and improve its electrophysical parameters. We have chosen, developed, and examined thoroughly the method of oxidation in oxygen glow discharge plasma [23] for precision generation of NO on the MCT surface.

It was demonstrated in our previous studies that an ultrathin NO with a thickness of just ~ 2 nm does indeed stabilize [24] and passivate efficiently the CdHgTe surface, forming a quality insulator−semiconductor interface (with aluminum oxide Al_2O_3 films fabricated by plasma-enhanced

atomic layer deposition (PE-ALD) [25] used as an insulator). An *n*-type semiconductor sensitive both in the middle (MWIR) and the far (LWIR) IR ranges was used to examine the influence of native MCT oxide on the electrophysical parameters of metal–insulator–semiconductor (MIS) structures. This semiconductor also had a so-called surface graded-gap layer (SGGL) with a thickness of 200–500 nm, which was characterized by a smooth increase in the molar fraction of cadmium telluride (i.e., increase in the band gap width) in the direction from the bulk to the surface and was expected to provide partial stabilization and passivation of narrow-band MCT [26].

In view of the fact that the fabrication of FPAs based on *p–n* junctions requires passivation of, first, both *p*- and *n*-type regions and, second, regions with and without (e.g., walls of mesa structures) an SGGL, the present study was aimed at fabricating MIS structures based on LWIR mercury cadmium telluride of different conductivity types and different surface compositions (with and without a surface graded-gap layer) and examining their electrophysical characteristics.

2. Experimental procedure

Heteroepitaxial *n*- and *p*-type LWIR $Cd_xHg_{1-x}Te$ structures with $x \approx 0.22$ in the working layer were fabricated by molecular beam epitaxy (MBE) at the Laboratory of Molecular Beam Epitaxy of $A^{II}B^{VI}$ Compounds (Institute of Semiconductor Physics, Siberian Branch of the Russian Academy of Sciences). An n^+-sublayer with a carrier density of $\sim 2.5 \cdot 10^{16}\,cm^{-3}$ was formed via doping with indium in the process of structure growth. It lay much lower than the working layer and provided an opportunity to reduce the series (bulk) resistance of the semiconductor material. The donor density in the undoped working layer determined using the Hall method was $\sim 5 \cdot 10^{14}\,cm^{-3}$. The samples grown with electron conductivity were subjected to annealing (vacancy doping) to obtain *p*-type samples with an acceptor density as high as $5 \cdot 10^{15}\,cm^{-3}$ in the working layer. MCT samples of both conductivity types grown with an SGGL (with a thickness of $\sim 0.4\,\mu m$ and x increasing to 0.45 on the surface) were divided into two parts, one of which was etched additionally in a polishing solution of bromine in hydrogen bromide in order to remove the SGGL chemically. CdHgTe samples of both conductivity types were also grown without an SGGL to analyze the influence of the process of chemical MCT etching on the electrophysical parameters of the insulator–semiconductor interface.

The surface of the studied MCT samples was cleaned chemically from native oxide formed during their storage in laboratory atmosphere by holding them for 30 min in ammonium hydroxide (NH_4OH) and rinsing two times with isopropyl alcohol. Immediately after cleaning, the samples were introduced into a vacuum gas-discharge chamber. To prevent plasma ions from affecting directly the semiconductor surface, the samples were positioned behind a solid anode. A glow discharge in oxygen atmosphere under a pressure of 0.15 Torr was sustained for 10 min under a voltage of 500 V; after that, the samples were removed from the chamber and transported immediately into an ALD setup. The resulting thickness of native MCT oxide was ~ 2 nm [23].

Aluminum oxide films with a thickness of 20 nm, which was monitored *ex situ* using a Woollam EC-400 spectral ellipsometer, were deposited onto all samples at a rate of ~ 0.5 nm/min in the Oxford FlexAl PE-ALD system. Trimethylaluminum ($Al(CH_3)_3$, TMA) was used as a precursor, and the substrate temperature was 120°C.

Gold contacts with an area of $6.9 \cdot 10^{-3}\,cm^{-2}$ were deposited onto the samples through a mask by thermal evaporation in vacuum. An Ohmic contact to the working layer/conducting MCT sublayer was established by scribing the sample end face and pressing an indium contact securely. The capacitance–voltage characteristics (CVCs, C–V) of the obtained MIS structures were measured with a WK 6440B LCR bridge meter; the samples were kept in a cryostat in darkness at liquid nitrogen temperature (77 K). The method for calculation of theoretical ideal CVCs (without the contribution of fast surface states) was similar to the one used in [27].

3. Experimental results and discussion

3.1. Capacitance–voltage characteristics of MIS structures based on *n*-CdHgTe

At liquid nitrogen temperature and a measurement signal frequency up to 1 kHz, all the obtained MIS structures based on *n*-type MCT have a characteristic low-frequency (LF) dependence of the capacitance on the gate bias (Fig. 1). As the frequency increases, the capacitance in inversion decreases (i.e., the transition from a low-frequency CVC to a high-frequency (HF) one occurs); however, the characteristic HF CVC shape was not observed even at the limit frequency of the measurement instrument (3 MHz). A positive fixed charge with density N_{fix} falling within the range of $(1–5) \cdot 10^{11}\,cm^{-2}$ is also a common feature of these structures.

It follows from Fig. 1 that structures with a surface graded-gap layer differ fundamentally from those without it both in the nature of variation of the surface potential and the electric capacitance of a semiconductor in transition from depletion to inversion (the capacitance minimum is broader) and in that a well-marked CVC hysteresis loop forms under cyclic gate voltage sweep. The authors of [28] have proposed an explanation for weaker hysteresis in structures based on MCT without an SGGL. They point out that the surface potential of a semiconductor with a wide-gap layer varies within a wider range under gate voltage sweep than the surface potential of a narrow-gap semiconductor, and this results in trapping of a greater number of carriers at slow surface states and is manifested

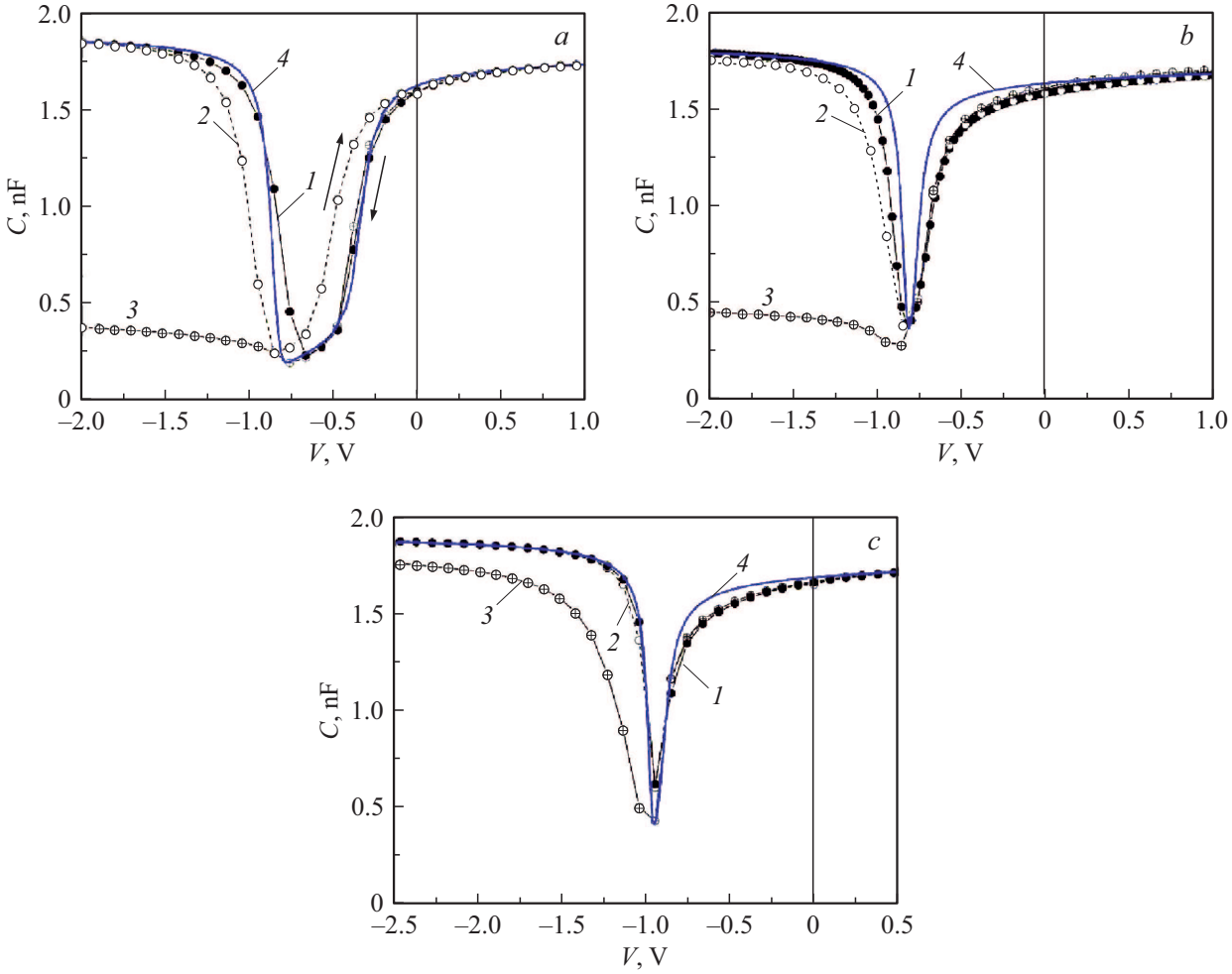

Figure 1. Capacitance–voltage characteristics of MIS structures Au–Al_2O_3–native oxide–n-$Cd_{0.22}Hg_{0.78}Te$ with a surface graded-gap layer (*a*) and without such a layer, which was either removed chemically (*b*) or not grown at all (*c*). Measurements were performed at a measurement signal frequency of 1 kHz (*1, 2*) or 1 MHz (*3*). Curves *1* and *2* demonstrate the dependence under cyclic voltage sweep (the sweep direction is indicated with arrows and remains the same in all plots). Curve *4* was obtained by numerical modeling.

in a wider CVC hysteresis. Thus, if we normalize the measured density of slow states to the bandgap width on the MCT surface for structures with an SGGL and without it, similar values on the order of $\sim 4 \cdot 10^{11}\,\mathrm{cm}^{-2} \cdot \mathrm{eV}^{-1}$ are obtained, which agrees with the proposed explanation.

Donor density N_D in the near-surface semiconductor region, which was adjusted in the process of plotting the theoretical CVC, was $\sim 5 \cdot 10^{14}\,\mathrm{cm}^{-3}$ for MCT samples grown with a surface graded-gap layer. This value is close to the data obtained in Hall measurements performed immediately after film growth. In the case of MCT grown without an SGGL, the donor density was higher: $N_D = 1.1 \cdot 10^{15}\,\mathrm{cm}^{-3}$.

The primary mechanism of enhancement of the donor density in MCT is the breaking of Hg–Te bonds, diffusion of interstitial mercury atoms, and their interaction with neutral defects/impurities of the crystal lattice (e.g., as a result of ion bombardment of the surface [29–31]). That said, the physicochemical process of formation of native MCT oxide is itself accompanied by breaking of Hg–Te bonds. However, since the glow discharge geometry with the oxidized sample positioned behind a solid anode was used, direct bombardment with high-energy plasma ions is unlikely, and the oxidation conditions were the same for all the studied samples. The exact cause of generation of donor centers remains unknown, but the fact is that CdHgTe films grown without an SGGL are characterized by an elevated sensitivity to external impacts. Apparently, the surface layer with an increased CdTe concentration or the layer of metallic tellurium formed as a result of SGGL etching provide sufficient stabilization of the MCT surface in the process of oxidation in glow discharge plasma.

The stretching of experimental capacitance dependences relative to the theoretical ones along the voltage axis suggests that the insulator–semiconductor interface with the surface MCT layer removed features a considerably higher density D_{it} of fast surface states. In addition, the density of slow surface states in these structures is also higher (up

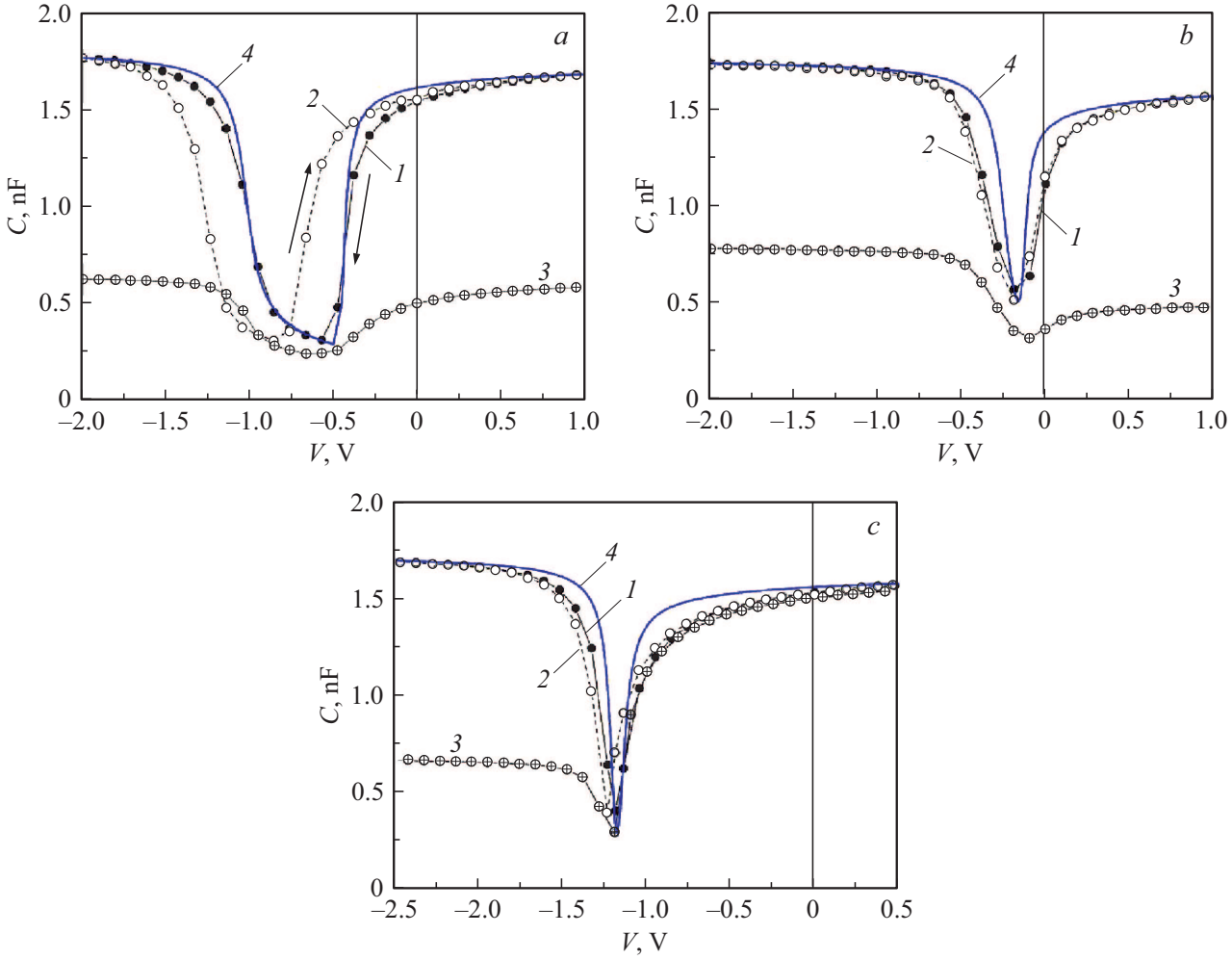

Figure 2. Capacitance–voltage characteristics of MIS structures Au–Al_2O_3–native oxide–p-$Cd_{0.22}Hg_{0.78}Te$ with a surface graded-gap layer (*a*) and without such a layer, which was either removed chemically (*b*) or not grown at all (*c*). Measurements were performed at a measurement signal frequency of 1 kHz (*1, 2*) or 1 MHz (*3*). Curves *1* and *2* demonstrate the dependence under cyclic voltage sweep (the sweep direction is indicated with arrows and remains the same in all plots). Curve *4* was obtained by numerical modeling.

to $1 \cdot 10^{12}\,cm^{-2} \cdot eV^{-1}$. These observations agree with the well-known assertions that MCT etching in bromine solutions has a negative effect on the electrophysical parameters of the interface [5]; the proposed passivation technique does not negate this effect.

The experimental characteristics of MIS structures based on unetched mercury cadmium telluride are fairly close to the ideal ones. The deviation (most pronounced in the samples without an SGGL) in the region of accumulation of the surface with majority charge carriers is attributable in part to the effects of band nonparabolicity and semiconductor degeneracy, which were not factored into the calculation model [4]. In the case of structures with a graded-gap layer, the experimental data also deviate from the theoretical ones in the region of depletion–weak inversion. The authors of [28] have noted that if a graded-gap layer is present on the $Cd_{0.22}Hg_{0.78}Te$ surface, the recharge time of surface states is so long that the capacitance–voltage characteristic is high-frequency relative to it (even if this characteristic is low-frequency relative to the lifetime of minority carriers). This implies that the observed deviation cannot be associated unambiguously with the contribution of capacitance of fast surface states to the resulting MIS capacitance. The combination of these factors renders the traditional (differential or integral) determination of the spectrum of surface states in these structures impossible.

3.2. Capacitance–voltage characteristics of MIS structures based on *p*-CdHgTe

Figure 2 presents the typical capacitance–voltage characteristics of metal–insulator–semiconductor structures fabricated based on MCT with hole conductivity after its oxidation in oxygen glow discharge plasma.

The fixed charge density in structures based on p-CdHgTe grown with a surface graded-gap layer (including the structures with an SGGL that was removed chemically afterwards) is $(1–6) \cdot 10^{11}\,cm^{-2}$, which is close to the

corresponding values for a semiconductor with electron conductivity. At the same time, the density of slow surface states is somewhat higher: $(6-8)\cdot 10^{11}\,\mathrm{cm}^{-2}\cdot\mathrm{eV}^{-1}$. The acceptor density estimated based on the capacitance in the minimum of low-frequency CVCs is $(4-6)\cdot 10^{15}\,\mathrm{cm}^{-3}$. The frequency dependence shows that the influence of series resistance in the measurement circuit, which is manifested in the frequency dispersion of capacitance both in inversion and in the region of accumulation of the surface with majority carriers, is much more pronounced in these structures. On the one hand, this is attributable to an increase in the bulk resistance of the semiconductor material due to a reduction in the mobility of majority carriers (holes). On the other hand, transformation of the equivalent circuit of the MIS structure aimed at isolating the series circuit resistance and correcting the measured capacitance of the structure [32] did not produce a meaningful result, thus indicating that the traditional equivalent circuit is inapplicable. The reason for this apparently lies in the specifics of donor compensation under vacancy doping of MBE n/n^+-CdHgTe structures and requires further study.

At low frequencies of the measurement signal, the experimental curves are similar in shape to the calculated ideal characteristics, although the degree of stretching is visually higher than the one in structures based on n-CdHgTe. This indicates that the density of surface states at the Al_2O_3/hole semiconductor interface is higher.

It follows from the frequency dependence of CVCs of structures based on MCT grown without a surface graded-gap layer that the near-surface semiconductor region features electron conductivity. In other words, the conductivity type is inverted. The estimated donor density is $1\cdot 10^{14}\,\mathrm{cm}^{-3}$; therefore, the donor increment is approximately the same for n- and p-type CdHgTe. These structures are also distinguished by an elevated $(1.1\cdot 10^{12}\,\mathrm{cm}^{-2})$ N_{fix} value. At the same time, it can be inferred that the lifetime of minority carriers in them exceeds the corresponding lifetime in the case when a semiconductor with an initially electron conductivity is used. This is evidenced by a more pronounced frequency dispersion of capacitance in inversion: a faster transition to the high-frequency pattern is observed at a lower measurement signal frequency. It is assumed that mercury cadmium telluride grown without a surface graded-gap layer features an excess density of bulk generation-recombination centers, which is neutralized in the process of subsequent vacancy doping (annealing).

4. Conclusion

MIS structures with ALD Al_2O_3 and an ultrathin native oxide on n- and p-$Cd_{0.22}Hg_{0.78}Te$ with a graded-gap layer and without it have been fabricated for the first time; their capacitance–voltage characteristics have been analyzed.

These structures feature a positive fixed charge with a density of $(1-6)\cdot 10^{11}\,\mathrm{cm}^{-2}$ and a relatively low density of slow states, which induce CVC hysteresis. It was demonstrated that, although the structures with a surface graded-gap layer have a more pronounced hysteresis, the ratio of the density of slow states to the surface band gap of the semiconductor material remains approximately the same.

The characteristics of MIS structures based on MCT with an SGGL are close in shape to the ideal theoretical ones. This indicates that fast surface states exert only a weak influence on the dependence of the surface potential on the bias voltage. The results of a qualitative comparative analysis demonstrate that the density of surface states increases following the removal of a surface graded-gap layer by etching in a bromine solution. This agrees with literature data and implies that the used passivation technique cannot ensure the formation of a quality interface of aluminum oxide with MCT after its etching.

Regardless of the surface composition, structures based on p-type MCT have higher densities of both slow and fast surface states. Therefore, coupled with the introduction of a positive fixed charge, the proposed passivation technique is more fitting for fabrication of „$p-$on$-n$“ photodiodes. With this configuration, a parasitic spatial charge region should not be present in the near-surface region of an electron semiconductor outside of the $p-n$ junction.

The surface structure of mercury cadmium telluride grown without a surface graded-gap layer is highly sensitive to the process of oxidation in oxygen glow discharge plasma. Oxidation results in the generation of donor levels and contributes to an increase in the magnitude of the positive fixed charge. The conductivity type is converted in a p-type semiconductor. The differences in frequency dispersion of the inversion capacitance of the structure suggest that the lifetime of minority carriers in CdHgTe grown without an SGGL and not subjected to post-growth annealing is significantly shorter.

The obtained results are of scientific and practical interest, since they reveal a pronounced positive effect of the proposed passivation procedure on the electrophysical parameters of MIS structures based on graded-gap LWIR CdHgTe ($x\approx 0.22$) of both conductivity types. The approach requires further development in terms of passivation of the MCT surface subjected to etching in a bromine solution.

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Conflict of interest

The authors declare that they have no conflict of interest.

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