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GaN field-effect transistor with efficient heat dissipation on Si substrate

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A simple design of a GaN field-effect transistor on a Si substrate with efficient heat removal through polydiamond layers formed on the walls of grounding holes is proposed. According to calculations, as a result of the introduction of such a heat sink with the same average distance between the gate sections, the maximum temperature in the channel of the GaN transistor on the Si substrate decreases significantly and becomes comparable to the maximum temperature in the channel of the GaN transistor on the SiC substrate..

Keywords: GaN FET, ground hole, channel temperature, polydiamond.

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Field-effect transistors based on gallium nitride heterostructures have a number of undeniable advantages that facilitated rapid progress in research into such transistors in recent years [1–4]. One of the key advantages of these heterostructures consists in their compatibility with SiC growth substrates, which have a very high thermal conductivity for a semiconductor material (estimated at $350-490\,\mathrm{W/(m\cdot K)}$ at a temperature of 300 K). The only physical constraint precluding one from exploiting the full potential of these substrates is the relatively low thermal conductivity of gallium nitride itself, which is roughly equal to $140\,\mathrm{W/(m\cdot K)}$. This translates into a considerable increase (30–40%) in the maximum temperature in the transistor channel even at a relatively small thickness of a GaN layer ($0.5\,\mu$m). However, the key advantage of the AlGaN/GaN heterostructure–SiC substrate complex (the mentioned high thermal conductivity of SiC) may also be regarded as the only serious problem on the way to wide adoption of such structures: SiC substrates are costly and have certain processing complexities associated with their fabrication. At first glance, this problem seems to be solvable without any substantial compromise in parameters by switching from $100\,\mu$m-thick SiC substrates to $50\,\mu$m-thick ones. However, this transition is virtually impossible to implement without a considerable increase in the distance between gate sections. The matter is that the thermal conductivity of silicon is approximately equal to $150\,\mathrm{W/(m\cdot K)}$, which is 2.3–3.2 times lower than the conductivity of silicon carbide. Depending on the transistor topology, a reduction in substrate thickness from 100 to $50\,\mu$m yields only a 10–20% reduction in thermal resistance instead of the desired value of 50%. This has a profound effect on the application prospects of silicon substrates.

In the present study, we propose a simple and effective method for improving the efficiency of heat removal from transistors that should eventually provide an opportunity to construct GaN transistors on Si substrates with a thermal resistance made sufficiently closer to the one of transistors on SiC substrates.

It is assumed that the topology of a power transistor is a standard one for devices of the millimeter wave range (Fig. 1). Figure 1 shows one transistor section (four gate and two drain sections). Two sections of this kind and five grounding holes are included into the calculation model. The obtained results demonstrate that the device temperature remains essentially unchanged when the number of sections is increased further.

Groups of gate and drain sections are separated in this design by octahedral source metallization sections. Through holes with side walls covered with grounding metallization are formed below the metallization of source sections in the heterostructure. Groups of gate and drain sections located between grounded sources then include only two gate sections and one drain section. Thus, only two heat output sources are located between two grounding holes in a transistor of this design.

The side walls of through grounding holes in the heterostructure are coated with an Au layer $1-5\,\mu$m in thickness. It is evident that this Au metallization of side walls of holes does not only establish an electric contact between source sections and the base of the transistor enclosure, but also serves (together with the region of heat transfer along the Si substrate) as a heat-sink element, although the efficiency of the Au heat bridge is fairly low due to the fact that the thermal conductivity coefficients of Au and Si are close. However, the pattern may change considerably if an additional diamond-like coating (DLC) [5–7] with a thermal conductivity of $500-1600\,\mathrm{W/(m\cdot K)}$ is applied to gold. It should be noted that the use of diamond coatings [8] and substrates [9] for cooling of transistors has already been proposed a number of times, but processing complexities stood in the way of commercial application of this approach, although the transfer of heterostructures to diamond substrates is an ultimate solution to the problem of heat removal.

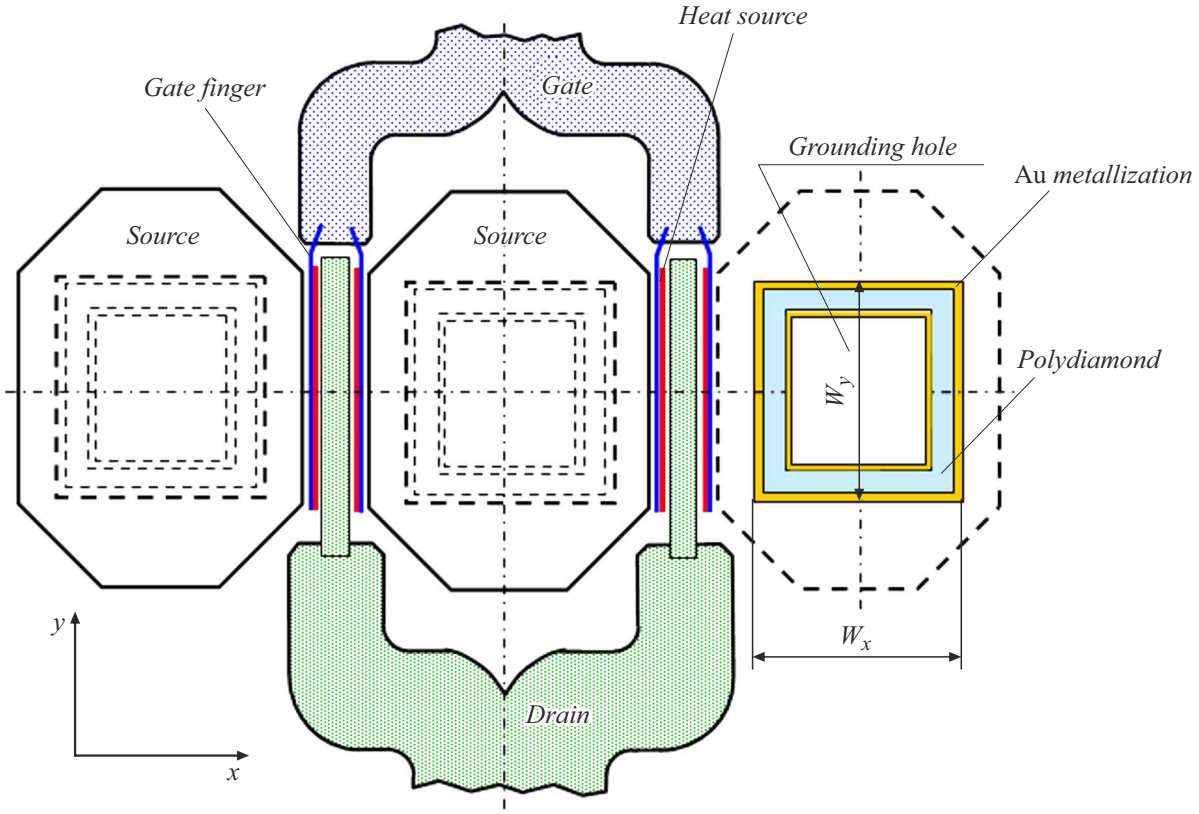

Figure 1. Schematic diagram of a group of sections of the transistor with a GaN channel (top view).

Two transistor designs were modeled: one had structure period $H = 60\,\mu$m and a distance of $15\,\mu$m between gates, and the other was characterized by $H = 45\,\mu$m and a distance of $10\,\mu$m between gates. Gate section width W was set to $150\,\mu$m, and the heat output was 5 W/mm, which corresponds to the same output power of 5 W/mm in continuous transistor operation with an efficiency of 50%. The temperature at the lower boundary of the Si substrate was assumed to be equal to 0°C. Since the device operation in the temperature region corresponding to insignificant degradation is of principal interest, temperature-independent thermal conductivity coefficients were chosen.

Figure 2 presents the maximum temperature in the transistor channel as a function of thickness of the heterostructure grown on a substrate for two indicated topologies at a SiC substrate thickness of $100\,\mu$m, thermal conductivities $\lambda = 490$ and $350\,\mathrm{W/(m \cdot K)}$, a Si substrate thickness of $50\,\mu$m, and a Si thermal conductivity of $150\,\mathrm{W/(m \cdot K)}$. These calculated data were obtained by solving numerically a three-dimensional steady-state heat conduction equation.

Grounding holes were not included into calculations of the dependences in Fig. 2. It can be seen that the maximum temperature for the design shown schematically in Fig. 1 in transistors on SiC substrates depends strongly on the net heterostructure thickness (together with the buffer) and increases by 30–55%. That said, it still remains significantly (1.5–2 times) lower than the maximum temperature in a transistor of the same topology on a Si substrate. It is hardly surprising that the latter temperature is virtually independent of the heterostructure thickness, since the thermal conductivities of Si and GaN are similar. The introduction of grounding holes coated with gold ($\lambda = 200\,\mathrm{W/(m \cdot K)}$) alters the pattern somewhat, although the change is far from being a fundamental one (Nos. 1–6 in the table).

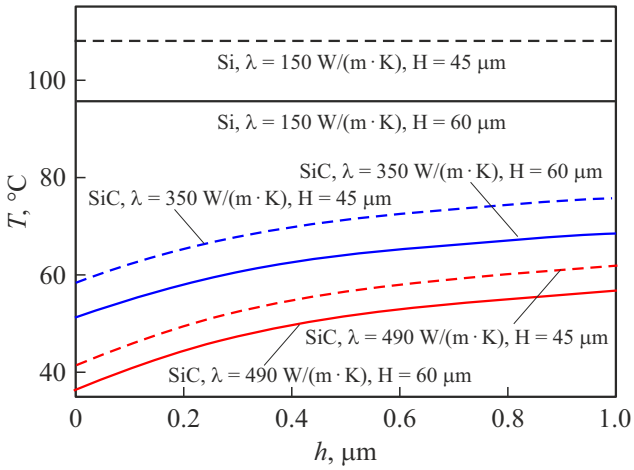

Figure 2. Dependence of the maximum temperature in the transistor channel on the net thickness of GaN/AlGaN layers grown on a substrate.

Maximum temperatures T in the transistor channel (the source (gate) width is $150\,\mu$m, and the power of each source is $750\,\mu$W)

№	Step, μm	Substrate			Hole $W_x \times W_y$, μm	Coating			T, °C
		Material	Thickness, μm	Thermal conductivity, W/(m·K)		Material	Thickness, μm	Thermal conductivity, W/(m·K)	
1	60	SiC	100	490 350	No	–	–	–	51.27 63.91
2	45	SiC	100	490 350	No	–	–	–	56.43 66.62
3	60	Si	50	150	No	–	–	–	95.76
4	45	Si	50	150	No	–	–	–	108.0
5	60	SiC	100	490 350	25 × 50	Au	5	200	55.24 68.73
6	45	SiC	100	490 350	15 × 50	Au	5	200	60.49 75.88
7	60	Si	50	150	35 × 130	Au DLC	1 5	200 1500	71.97
8	45	Si	50	150	25 × 130	Au DLC	1 5	200 1500	74.39
9	45	Si	50	150	25 × 130	Au DLC	1 5	200 1000	81.78
10	45	Si	50	150	25 × 130	Au DLC	1 5	200 500	97.519
11	45	Si	50	150	25 × 130	Au DLC	1 10	200 500	83.09
12	45	Si	50	150	25 × 130	Au DLC	1 10	200 1000	71.03
13	45	Si	50	150	25 × 130	Au DLC	1 10	200 1500	65.99
14	45	SiC	100	490 350	25 × 130	Au DLC	1 5	200 1500	56.26 64.97

The maximum temperature in transistors on SiC substrates increases slightly (approximately by 10%). A substantial change is observed when a diamond-like coating with a high thermal conductivity and uniform thickness (Nos. 7, 8) is deposited on top of a thin gold layer ($1\,\mu$m in calculations) in grounding holes of transistors on Si substrates. The maximum device temperature decreases markedly in this case, dropping to a level corresponding to the maximum temperature in transistors on SiC substrates with grounding holes (Nos. 5, 6).

However, it should be noted that this enhancement of heat removal efficiency in devices on Si substrates imposes rather strict requirements as to the DLC quality: a reduction in thermal conductivity of these coatings translates into a substantial increase in the maximum transistor temperature (Nos. 8–10). However, this drawback may be mitigated by the application of a thicker coating (Nos. 11–13). At the same time, owing to a high thermal conductivity of silicon carbide, the introduction of a DLC in grounding holes of transistors on SiC substrates results only in a minor temperature reduction (Nos. 6, 14).

The methods of magnetron sputtering of carbon or plasma-enhanced chemical vapor deposition [5,10] ensure a sufficiently low processing temperature (no higher than 300°C) and are thus well-suited for the application of diamond-like coatings to the Au metallization of walls of grounding holes. The CVD process involving the decomposition of hydrocarbons mixed with hydrogen and subsequent deposition of diamond onto a heated substrate [6] is used to deposit DLCs. The working mixture of gases dissociates in a vacuum chamber under the influence of microwave plasma; the gas pressure in the chamber is 30–100 Torr, and the deposition rate is $10-20\,\mu$m/h. The characteristic thermal coefficient of linear expansion of diamond

$((9-5)\cdot 10^{-7}{}^{\circ}\mathrm{C}^{-1})$ is almost an order of magnitude lower than the corresponding coefficient of gold $(14\cdot 10^{-7}{}^{\circ}\mathrm{C}^{-1})$. This is the reason why the DLC–Au contact is effected via an adhesion layer (titanium, tantalum, titanium carbide) with a high carbon affinity that forms high-adhesion joints with it in vacuum or inert atmosphere [7]. A window needed to establish contact between the solder and the metallization of the back of the substrate is then opened by photolithography in the DLC covering the back of the substrate.

The obtained results demonstrate that, in certain scenarios, the deposition of diamond-like coatings onto walls of grounding holes is an efficient method for reducing the maximum temperature in the channel of field-effect transistors based on gallium nitride heterostructures grown on Si substrates. The channel temperature in such devices may be close to the channel temperature of transistors on SiC substrates.

However, if a way to produce thinner heterostructures on SiC substrates for GaN transistors without the associated reduction in mobility and surface density of electrons should be found, these structures shall be unparalleled in terms of efficiency of heat removal regardless of the transistor topology.

Conflict of interest

The authors declare that they have no conflict of interest.

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