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Forming regimes of Pd/Ge/Au contact system to *n*-GaAs influence on its electric parameters

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The investigations of Pd/Ge/Au contact system forming regimes influence on the specific contact resistivity to *n*-type conductivity GaAs layer were carried out. The method of samples surface treatment before the layers evaporation and thermal annealing regimes in H_2, N_2 and Ar atmosphere influence on contact system parameters was investigated. The specific contact resistivity value $(2-3) \cdot 10^{-6}$ Ohm$\cdot$ cm^2 at the reduced annealing temperature 190°C was archived..

Keywords: Pd/Ge/Au, *n*-GaAs, surface treatment, thermal annealing

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The advancement of semiconductor device technology (including the technology of photovoltaic converters of power radiation) contributes to increases in the device efficiency and power, thus necessitating the strengthening of requirements imposed on the processes of fabrication of heterostructures, Ohmic contacts, and protective and antireflective coatings [1–4]. The development of Ohmic contact systems facilitates a reduction in resistive loss by suppressing the contact resistivity and enhancing the conductivity of contact systems. This, in turn, leads to a reduction in the series resistance of semiconductor devices [5,6].

A multilayer Au(Ge)/Ni/Au contact, which provides contact resistivity $\rho_c \approx 10^{-6}\,\Omega\cdot\text{cm}^2$ [7], is a widely used contact system for *n*-type GaAs layers. However, the process of fabrication of an Au(Ge)/Ni/Au Ohmic contact involves high-temperature ($T > 370$°C) annealing performed for several minutes. This entails uneven fusion of contact system components into the semiconductor material, thus exerting a negative influence on the contact morphology and shaping a non-uniform distribution of the contact resistance over the sample area. If such contact systems are used to produce semiconductor devices with a shallow $p-n$ junction, their electric characteristics may be impaired significantly. A Pd/Ge/Au contact system for *n*-type GaAs layers is an alternative to a multilayer Au(Ge)/Ni/Au contact. This system provides contact resistivity $\rho_c \approx 10^{-6}\,\Omega\cdot\text{cm}^2$ at a thermal annealing temperature below 200°C [8,9].

The aim of the present study is to analyze and optimize the process of fabrication of Ohmic Pd/Ge/Au contacts to *n*-type GaAs layers under reduced thermal annealing temperatures and examine the influence of the method of sample surface treatment before the deposition of palladium, germanium, and gold layers and of the regimes of thermal annealing in H_2, N_2, and Ar atmosphere on the electric parameters of a contact system.

This research into the technology of fabrication of Pd/Ge/Au contact systems was carried out using test samples fabricated from a structure containing a 150 nm-thick *n*-GaAs layer doped with Si (with a free electron density of $2 \cdot 10^{18}\,\text{cm}^{-3}$) grown on a semi-insulating GaAs substrate. Rectangular contact pads positioned at different distances from each other were formed on test samples. The material around groups of contact pads was etched down to the semi-insulating GaAs substrate to suppress the effects of edge surface current spreading. The contact resistivity was measured using the TLM (transmission line model) method with a rectangular (linear) geometry of contact pads (linear TLM, LTLM) [9].

Bus-bars on test samples were formed using lift-off photolithography with LORs (lift-off resists). A T-shaped profile of side walls of the resist (Fig. 1) made it possible to create gaps between the material deposited onto a semiconductor

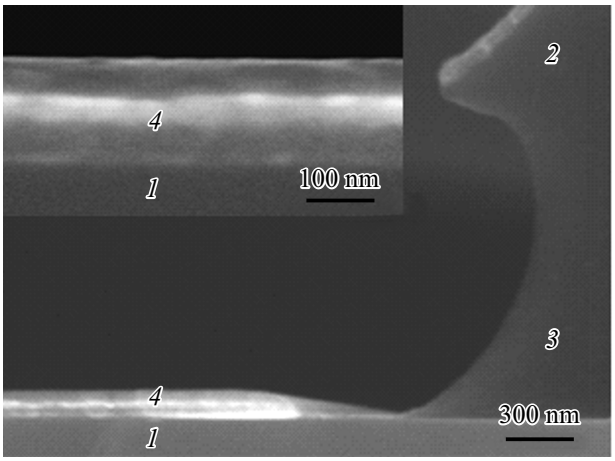

Figure 1. Heterostructure cleavage imaged with a scanning electron microscope. *1* — Heterostructure, *2* — photoresist mask, *3* — LOR sublayer, *4* — deposited Pd/Ge/Au.

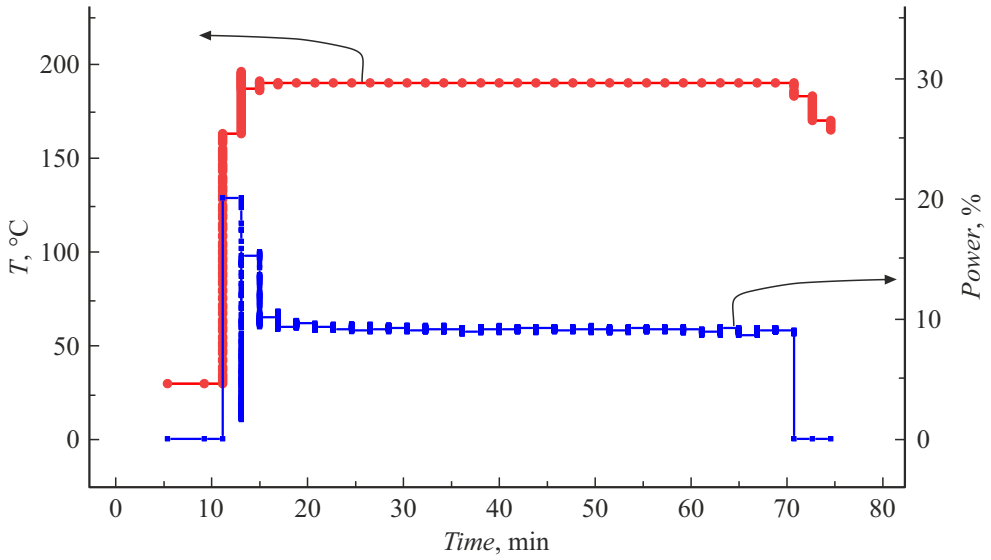

Figure 2. Regime of thermal annealing in N_2 or Ar atmosphere at STE RTA100.

and onto the photoresist mask, thus facilitating its removal and providing for the formation of bus-bars with plane walls. The use of LOR layers ensures high stability of the lift-off photolithography process in deposition of thick metal films. This provided an opportunity to fabricate device structures without any additional electrolytic contact thickening.

Layers were deposited by resistive evaporation of Pd and Ge from tungsten boats and Au from a molybdenum boat in vacuum. Samples were annealed in the atmosphere of H_2 (purified with a palladium filter), N_2, or high-purity Ar. Annealing in a flow of N_2 and Ar was performed using an STE RTA100 rapid thermal annealing system. Figure 2 presents one of the sample annealing regimes: processing for 60 min at a temperature of 190°C. Rapid stabilization of the thermal annealing regime and temperature holding were achieved by adjusting the heater power: it was set to approximately 20% of the maximum (~ 27 kW) at the first stage and reduced to 7–9% later on. Annealing in a hydrogen flow was performed in a tube-type quartz reactor with a similar profile of heating (4–8 min), temperature holding, and rapid cooling.

Preparatory processing of the surface of a semiconductor heterostructure exerts a significant influence on the morphology and adhesion of deposited layers and on the electric parameters of devices being produced. Immediately prior to the deposition of a contact system, the surface of test samples was processed to remove the layer of natural GaAs oxides by ion-beam etching (with argon ions) or wet chemical etching in diluted hydrochloric acid. Argon etching ensures a high surface preparation grade, thus normally facilitating adhesion of deposited coatings. However, since material is removed as a result of mechanical separation of atoms of surface GaAs layers under bombardment by heavy Ar atoms, a defect damaged layer with a thickness of several nanometers forms in the process. This layer interferes with the formation of a Pd/Ge/Au contact to *n*-GaAs with low contact resistivity values at low annealing temperatures. With annealing temperatures of 185–210°C, H_2 atmosphere, and a process duration of 30–60 min, the values of contact resistivity remained at the level of $\rho_c \approx 10^{-3}\,\Omega \cdot \mathrm{cm}^2$. This may be attributed to the fact that contact material layers do not fuse into the semiconductor surface at low annealing temperatures; thus, a defect damaged layer in the near-contact region exerts a negative influence on the contact conductivity. At an elevated annealing temperature of 400°C, fusion of contact system materials into the *n*-GaAs surface was achieved, and the negative effect of the damaged layer was neutralized: the values of contact resistivity dropped to $\rho_c \approx 10^{-5}\,\Omega \cdot \mathrm{cm}^2$.

Wet chemical etching in diluted HCl is an alternative method of GaAs surface processing that ensures efficient removal of the natural GaAs oxide layer and provides an opportunity to form an Ohmic contact with fine adhesion to the heterostructure surface and a low contact resistivity ($\rho_c \approx 10^{-6}\,\Omega \cdot \mathrm{cm}^2$).

The thickness of the palladium layer adjacent to the *n*-GaAs semiconductor structure material has a significant effect on the parameters of the Pd/Ge/Au contact system. Figure 3 presents the results of LTLM measurements of contact resistivity for different contact system types with thermal processing in hydrogen atmosphere within a wide temperature range ($T = 185$–400°C). The highest reproducibility and the lowest values of contact resistivity are achieved at a Pd layer thickness of 10–20 nm (Ge 30 nm and Au 100–150 nm) layer thicknesses were fixed at the levels determined in earlier studies [7]): $\rho_c \approx 10^{-6}\,\Omega \cdot \mathrm{cm}^2$ at $T = 185$, 210°C and $\rho_c \approx 10^{-5}\,\Omega \cdot \mathrm{cm}^2$ at $T = 290$°C (annealing for 30–60 min in hydrogen atmosphere). If the Pd layer thickness changes, the ratio of Ge and Pd thicknesses varies accordingly, and ρ_c increases as a result

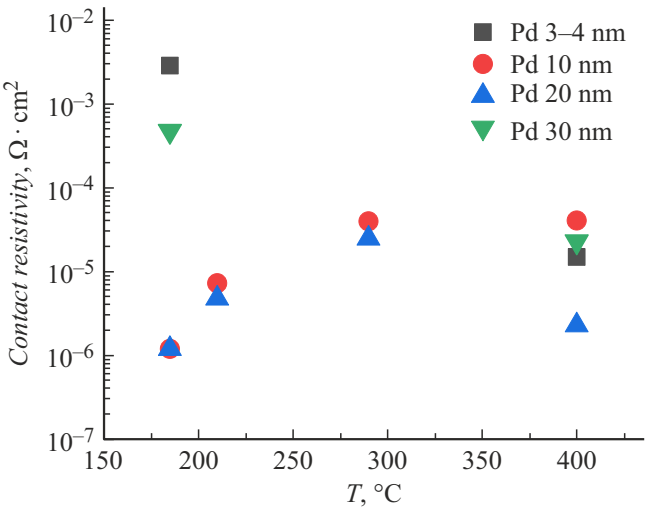

Figure 3. Dependence of the contact resistivity of a Pd/Ge/Au Ohmic contact on the annealing temperature (in hydrogen atmosphere) at a Pd thickness of 3–30 nm.

by more than an order of magnitude at low annealing temperatures. This is likely due to the fact that new compounds (PdGe, Pd_2Ge, PdGa, Pd_2Ga, $PdAs_2$, GeAs, $GeAs_2$, etc.), which may have different conductivities, are produced in the process of annealing of a contact structure with different Ge/Pd ratios and become dominant in the bulk of the contact. When the amount of Ge in contact layers is slightly higher than the amount of Pd, ρ_c decreases; in our view, this is attributable to the crystallization of an epitaxial layer of narrow-band „excess" Ge on the GaAs surface from solid solution PdGe that is produced when the contact is heated [10]. However, when the Pd layer thickness decreases to 3–4 nm, the conditions for production of palladium germanide with a thickness needed for Ge epitaxy on the GaAs surface are not fulfilled. The contact system is then formed mostly by amorphous Ge and Au layers following after palladium, and the annealing temperature needs to be increased considerably (to 400°C) in order to obtain low contact resistivity values. When the Pd layer thickness increases to 30 nm, the diffusion of Ge to the GaAs surface is suppressed; a contact system of the needed composition does not form, and the contact resistivity increases as a result.

At a annealing temperature 400°C, the effect of the Pd layer thickness on the electric parameters of a contact is neutralized due to fusion of Ge and Au into the *n*-GaAs surface; thus, the contact resistivity at high annealing temperatures is almost independent of the palladium layer thickness.

According to the obtained results, the optimum annealing regime for the studied contact is processing at a temperature of 190°C for 60 min. The retrieved data were used to examine the influence of gas atmosphere (H_2, N_2, and Ar) in the process of annealing on the contact system parameters. The minimum values of contact resistivity

Effect of the annealing atmosphere (at $T = 190$°C, $t = 60$ min) on the contact resistivity

Atmosphere	Contact resistivity, $\Omega \cdot cm^2$
H_2	$2 \cdot 10^{-6}$
N_2	$3 \cdot 10^{-6}$
Ar	$3 \cdot 10^{-5}$

$\rho_c \approx (2-3) \cdot 10^{-6}\ \Omega \cdot cm^2$ were achieved in annealing in H_2 and N_2 atmosphere (see the table). Lower contact resistivity values are normally obtained in annealing of a Pd/Ge/Au contact in hydrogen atmosphere [9], since a Pd film becomes enriched with molecular hydrogen, which dissociates in the process of dissolution. Atomic hydrogen present in a palladium layer then reduces Ga_2O_3 on the GaAs surface, thus facilitating a reduction in contact resistivity.

The following optimum regimes and parameters of fabrication of a Pd/Ge/Au contact system for *n*-GaAs were determined in the present study: sample surface processing in diluted hydrochloric acid prior to deposition, a Pd layer thickness of 10–20 nm with a Ge layer thickness of 30 nm, and contact annealing at a temperature of 185–190°C for 60 min in H_2 or N_2 atmosphere. The lowest contact resistivity values achieved for Pd/Ge/Au and *n*-GaAs were $\rho_c \approx (2-3) \cdot 10^{-6}\ \Omega \cdot cm^2$.

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Conflict of interest

The authors declare that they have no conflict of interest.

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