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The effect of surface traps on the static characteristics and the saturation current spread in the channel of GaN HEMTs

© V.G. Tikhomirov[1], S.V. Chizhikov[2], A.G. Gudkov[2], V.M. Ustinov[3]

[1] St. Petersburg State Electrotechnical University „LETI", St. Petersburg, Russia
[2] Bauman Moscow State Technical University, Moscow, Russia
[3] Submicron Heterostructures for Microelectronics, Research & Engineering Center, RAS, Saint-Petersburg, Russia
E-mail: greenbob54@gmail.com

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The article discusses the method of neutralization of surface traps in the structures of gallium nitride transistors with high electron mobility (GaN HEMT), based on the use of step-by-step temperature exposure — thermal training. Calculations and experimental studies of the effect of traps on the static characteristics of GaN HEMT have been carried out, and effective ways of dealing with traps have been proposed, in particular, using the proposed optimal thermal training modes.

Keywords: surface traps, HEMT, GaN.

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$A^{III}B^{V}$ heterostructures based on gallium arsenide are currently being replaced in microwave electronics (primarily in the role of materials for energy-efficient transistors, which may be used in the amplification section of microwave equipment) by heteroepitaxial group III nitride structures. High levels of electron density in the channel and breakdown voltage provide an opportunity to raise the power density in microwave field-effect GaN transistors by a factor of 5−10 relative to similar GaAs devices. Several problems also emerge in operation of gallium nitride high-electron-mobility transistors (GaN HEMTs) in microwave regimes. One of them consists in the presence of defects of various types, which exert a profound negative influence on both the speed performance and the output power of a device, in the transistor structure [1]. The effect of surface traps, which emerge at the interface between thin passivating dielectric (e.g., Si_3N_4) layers and the barrier AlGaN layer, on the operation of nitride HEMTs is especially significant. In view of this, the ways to moderate the influence of these traps on device parameters are being actively searched for. A method for neutralization of surface traps via step-by-step temperature exposure (thermal training) is examined in the present study. The effect of traps on static characteristics of transistors is calculated and studied experimentally, and efficient methods for managing these traps are proposed.

Several GaN/AlGaN heterostructures were grown for experiments by MOCVD (metalorganic chemical vapor deposition) on SiC substrates, and HEMTs with a T-shaped gate 200 μm in width and 0.5 μm in length (these parameters are dictated by their frequency operation range) were fabricated based on the prepared samples. The key functional layers of the transistor heterostructure are the buffer GaN layer 2 μm in thickness and the barrier $Al_{0.23}Ga_{0.77}N$ layer with a thickness of 20−22 nm. Silicon nitride produced by deposition in plasma under electron cyclotron resonance conditions was the dielectric material positioned below the „head" of the T-shaped gate. Lift-off lithography was used for Ohmic contact metallization and the layout of contact pads. A Ti/Al/Ni/Au metallization system with subsequent rapid thermal annealing in nitrogen was used for Ohmic contacts. Inter-device insulation was established by ion implantation. Ni/Au gate metallization was formed by electron-beam lithography and thermal evaporation. The results of preliminary examination of these transistors were detailed in [2]. A wafer with fabricated transistors was divided into separate chips, and reference samples for subsequent experiments were chosen according to the following criteria: a saturation current of 160–190 mA, a cutoff voltage no lower than 5 V, and a leakage current no greater than 300 μA at a gate−drain voltage of 60 V (these criteria follow the suitability requirements outlined in the design specification).

HEMTs were subjected to extensive testing that involved the examination of all key characteristics and the determination of operating parameters. Specifically, we determined their power parameters, delay times, saturation currents, etc. Particular attention was paid to the identification and examination of traps in prepared transistor structures with a passivating dielectric and the evaluation of their influence on the operating characteristics of devices. The procedure of these experiments involved the activation of traps by optical irradiation at a photon energy of 1.0–4.5 eV. The characteristic energies of photons activating the traps were determined, and the relative output power increment and relaxation times of surface traps were calculated. A method for neutralization of surface traps, which provides an opportunity to suppress their influence, was proposed. This method involves a single (or step-by-step) exposure of

structures to elevated temperatures (from 200 to 350°C). The overall exposure time varied from several minutes to 8 h.

In order to analyze the effect of traps on the output characteristics of a transistor, its characteristics were simulated with the use of already available and tested numerical HEMT models [2–4] that incorporated calibrations and numerical algorithms for heterostructure calculations (models of traps included) [5,6]. Following the adaptation of mathematical models to the fabricated transistor specifics (i.e., the assumed presence of traps in different structural regions), a numerical experiment into the potential influence of emergence and positioning of traps in the transistor structure on current–voltage curves (CVCs) of GaN HEMTs was carried out. A transistor structure without traps was specified for this purpose within the developed model, and CVCs were calculated. Virtual traps with the most probable characteristics, which were taken from literature and verified by the results of our own experiments, were then introduced into their presumed locations. The results of modeling were verified by experimental data on the output parameters of transistors.

It should be noted that the emergence of mobile charges at the GaN/AlGaN interface in the examined nitride transistor heterostructure is associated directly with the effects of spontaneous polarization and piezoelectric polarization, which manifest themselves in a wurtzite-type crystal lattice; this is a fundamental distinction between it and heterostructures based on gallium arsenide. The resulting complex equilibrium distribution of a system of charges, which includes the charges of traps in the buffer, in the barrier layer, and at the semiconductor–dielectric interface, from the heterostructure surface to the substrate induces the formation of a quantum well (filled with a two-dimensional high-mobility and high-density electron gas) at the heteroboundary. The schematic diagram of the depth distribution of charges in the heterostructure is shown in Fig. 1. The following quantities are indicated: $+\sigma_s$ is the immobile positive charge on the heterostructure surface; $-\sigma_{\mathrm{AlGaN}}$ is the immobile negative charge of the barrier layer associated with the effects of spontaneous and piezoelectric polarization; $-\sigma_{\mathrm{GaN}}$ is the immobile negative charge at the boundary between buffer and barrier layers associated with the effects of spontaneous and piezoelectric polarization; $+\sigma_{\mathrm{AlGaN}}$ is the immobile positive charge of the barrier layer associated with the effects of spontaneous and piezoelectric polarization; and $-qn_s$ is the mobile negative charge near the boundary between buffer and barrier layers associated with carriers in the transistor channel.

It becomes clear in view of the above that traps may exert a very significant influence on the output characteristics of a heterostructure GaN/AlGaN transistor. In addition, such electron states extending to the barrier layer surface may exacerbate the problems induced by a large number of nitride dangling bonds present on the heterostructure surface after its removal from the growth chamber. As the electric field strength increases in the course of transistor

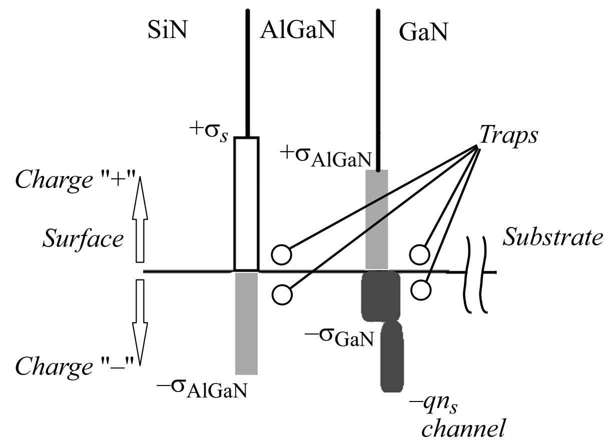

Figure 1. Diagram of the depth distribution of charges and the probable positioning of traps in the nitride transistor heterostructure.

operation, the height of the barrier through which a trapped electron may tunnel decreases due to the Poole–Frenkel effect [7]. Therefore, electrons trapped near the Fermi level may migrate easily to surface traps, thus exerting a more profound influence on the static and dynamic transistor characteristics. The traditional method for suppression of these effects is the application of a passivating SiN film coating to the nitride heterostructure surface. A marked reduction in the density of surface states is normally observed after passivation. However, it should be noted that while SiN passivation reduces the density of traps on the surface, it cannot remove traps completely. The initial surface state prior to passivation, the SiN film quality, the conditions and regimes of film deposition, and other technological and design parameters of a transistor are crucial here.

It is normally assumed that a fine transistor performance may be achieved by cleaning the wafer surface with acetone and ethanol and subjecting it to acid treatment (hydrochloric acid diluted with water at a ratio of 1:5) prior to the introduction of this wafer into the chamber for SiN film deposition. Before the deposition, the temperature in the chamber is raised to 300°C, which is 50°C higher than the SiN film deposition temperature, and the wafer is held for 40 min in a nitrogen atmosphere.

However, our research indicates that the influence of surface states on the static characteristics of a transistor still remains significant if thermal training is not performed.

Calculations were carried out for several typical trap parameters and locations, and transistor CVCs were obtained for each variant. These calculated CVCs were then compared to the experimental ones measured before and after annealing in air at a temperature of 300°C for 3 h. If these CVCs align within the predetermined error limit (normally set to several percent), it is fair to assume that traps probed in the experiment are located at spots specified in numerical simulations and have the presumed parameters.

The results of numerical modeling and their comparison with experimental data are presented in Fig. 2.

It follows from Fig. 2 that CVCs calculated without regard to the influence of traps agree well with the experimental curves for transistors annealed at 300°C for 3 h. In the case of non-annealed transistors, a fine agreement with experimental data is provided by the model that includes traps with certain parameters. The closest agreement is achieved when traps are located at the dielectric–semiconductor boundary. It should be noted that the CVCs of transistors did not change in any significant way after annealing at temperatures lower than 300°C (200–250°C), and prolonged annealing for 5–8 h also did not result in any noticeable enhancement of the channel current (relative to thermal processing at 300°C for 3 h). The regimes of annealing at temperatures much higher than 300°C lead to gate degradation and are inapplicable in the present case. The following trap parameters were set: an activation energy of 1.7 eV, a surface density of $5 \cdot 10^{13}\,\mathrm{cm}^{-2}$, and a capture cross section of $5 \cdot 10^{-19}\,\mathrm{cm}^2$. If the influence of thermal stabilization on the dynamics characteristics of a device needs to be evaluated, the most accurate results in a numerical experiment are obtained when traps in the buffer layer with an activation energy of 1.8 and 2.5 eV, a density of $1 \cdot 10^{17}\,\mathrm{cm}^{-3}$, and a capture cross section of $4 \cdot 10^{-16}\,\mathrm{cm}^2$ and traps in the barrier layer with an activation energy of 2.9 eV, a density of $1 \cdot 10^{17}\,\mathrm{cm}^{-3}$, and a capture cross section of $4 \cdot 10^{-16}\,\mathrm{cm}^2$ are taken into account. This agrees well with the data from [5] and the results of studies reported in [6–10].

The estimates obtained in numerical modeling suggest that the boundary between the barrier layer and the passivating dielectric layer is the area where traps are most likely to be found in the transistor structure. These traps are modified significantly in 3 h of annealing at a temperature of 300°C, which has a positive effect on the static transistor CVC.

The presented numerical modeling data are not oriented specifically at the calculation of output microwave characteristics and evaluation of changes in the output transistor power. Mathematical models incorporating the dynamic behavior of traps are needed for these purposes [11–13]. However, the presented results highlight those topological and technological features of a device that are important for improving the static output characteristics. A significant enhancement of the performance of fabricated transistors was achieved by applying the proposed annealing procedure. Specifically, the variation of the maximum channel current decreased several-fold (from 8.5 to 2.6 mA), and other device parameters were stabilized (e.g., the mean channel current increased from 166 to 193 mA). The obtained research data helped determine the optimum regimes of thermal training needed to achieve the best parameters of the examined HEMTs. This is illustrated by Fig. 3 that presents the maximum channel current levels measured before and after annealing for nine HEMTs subjected to thermal processing at 300°C for 3 h. It is evident that crucial

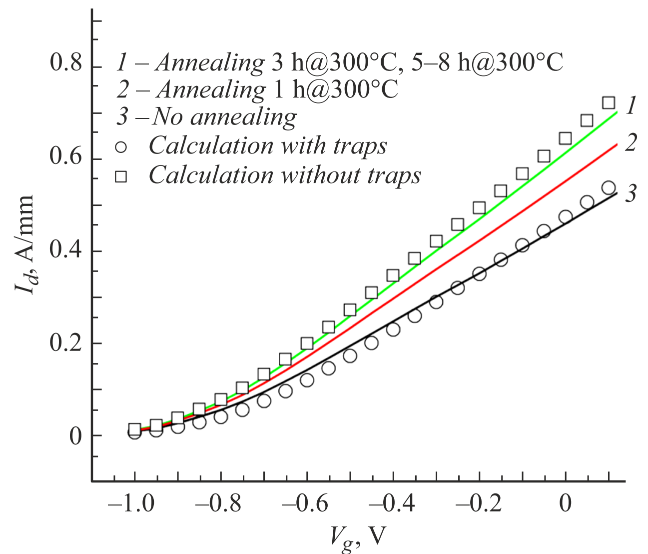

Figure 2. Experimental and calculated transfer current–voltage curves of the transistor corresponding to different thermal training regimes. Circles and squares denote the calculated data obtained with and without regard to the influence of traps. *1* — Experimental curve corresponding to thermal training at 300°C for 3 h (or more), *2* — experimental curve corresponding to thermal training at 300°C for 1 h, and *3* — experimental curve measured before annealing.

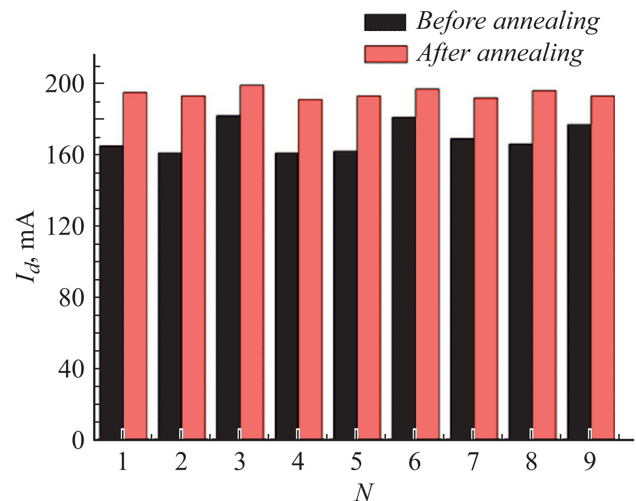

Figure 3. Maximum channel currents for the examined GaN/AlGaN HEMT samples before and after thermal training. The standard deviation before and after annealing is 8.5 and 2.6 mA, respectively. The mean value is 166 and 193 mA, respectively.

device parameters are stabilized (specifically, the spread of channel currents becomes much less pronounced, and the saturation current itself increases notably).

HEMTs based on GaN/AlGaN heterostructures with a T-shaped gate 200 μm in width and 0.5 μm in length featuring a thin Si_3N_4 passivating dielectric layer were

fabricated and studied. The key characteristics of transistors were examined, and their operating parameters (power, saturation currents, etc.) were determined. The influence of surface traps on the characteristics of transistors was examined theoretically via numerical modeling, and the obtained data were compared to experimental ones. It was demonstrated that traps located at the boundary between the AlGaN barrier layer and the Si_3N_4 passivating layer play an essential role. A method for neutralization of traps via thermal training at a temperature of 300°C for 3 h was developed. A significant enhancement of the performance of transistor structures was achieved by applying this procedure; specifically, the channel currents were stabilized markedly with the current spread decreasing from 8.5 to 2.6 mA (i.e., by a factor of 3).

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Conflict of interest

The authors declare that they have no conflict of interest.

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