Field p-channel transistors based on GaN/AlN/GaN heterostructures on a silicon substrate

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Various types of p-channel field-effect transistors based on GaN/AlN/GaN heterostructures are considered. The channel is formed by a polarization-induced two-dimensional hole gas. It is shown that the highest values of saturation current and transconductance are observed in a transistor with a gate formed by a two-dimensional electron gas from the side of the substrate.

Keywords: AlN/GaN heterostructure, two-dimensional hole gas, p-channel transistor, polarization.

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1. Introduction

Gallium nitride technology has great potential in power electronics [1]. Currently discrete n-channel transistors with high electron mobility (HEMT) with breakdown voltages up to 1 kV are created based on Al(Ga)N/GaN heterostructures which can replace the silicon hardware components in electric power conversion circuits, increasing efficiency and increasing power density [2].

At the same time, the monolithic integration of a high-power transistor and control modules, primarily the gate driver, is complicated by the lack of p-channel transistors for building energy-efficient complementary logic circuits. Attempts are being made to circumvent this limitation using alternative logic schemes, such as direct-coupled logic (DCFL) based on n-channel HEMT [3]. However, it has limitations related to low output currents, complex manufacturing processes and high temperature sensitivity.

The development of a p-channel transistor based on GaN was carried out less intensively than the development of n-channel transistor, since the mobility of holes in a layer of two-dimensional gas at room temperature is limited by acoustic scattering of phonons and does not exceed $\sim 25\,\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$ [4]. The low drift velocity of the holes prevents the creation of low-power, high-speed logic circuits competing with silicon. However, this velocity allows for monolithic integration of control circuits and power switches on a single chip, since typical operating frequencies of power conversion circuits are in the range from 100 kHz to 10 MHz. In addition to logic circuits, p-channel transistors can be used as an active load in analog circuits.

Various designs of p-channel field-effect transistors based on GaN/AlN/GaN heterostructures on a silicon substrate are discussed in this paper. Initially, AlN/GaN structures were used to manufacture n-channel transistors with high currents and transconductance. When an additional layer of GaN is built up, a two-dimensional hole gas is produced on the surface of AlN, which provides a technological basis for manufacturing p-channel transistors and monolithic complementary logic circuits.

2. Selecting model parameters

Crystals of metal nitrides of the III group have a hexagonal structure of the wurtzite type and are usually grown along the [0001] direction. Axis c of the hexagonal lattice is polar. As a positive direction, it is customary to choose the direction from the cation to the anion. The vector of spontaneous polarization $\mathbf{P}_{\mathrm{SP}}$ is directed along the axis c. A large spread of calculated values of spontaneous polarization is noted in [5,6] and the values $-0.034\,\mathrm{C/m}^2$ for GaN and $-0.09\,\mathrm{C/m}^2$ for AlN are recommended.

The permanent lattices of metal nitrides of the III groups differ from each other. Therefore, in addition to spontaneous polarization, it is also necessary to take into account the piezoelectric polarization $\mathbf{P}_{\mathrm{PE}}$ associated with the deformation of the material:

$$\mathbf{P} = \mathbf{P}_{\mathrm{SP}} + \mathbf{P}_{\mathrm{PE}}.$$

The relation connecting the polarization along the axis c and the tensor of elastic modules of the material in Voigt's notation has the following form [7]:

$$P_{\mathrm{PE}} = 2\,\frac{a - a_0}{a_0}\left(e_{31} - e_{33}\,\frac{C_{13}}{c_{33}}\right),$$

where C_{13} and C_{33} — components of the tensor of elastic modules of the material, e_{33} and e_{31} — piezoelectric coefficients. The relationship between them is such that the contribution to polarization associated with the piezoelectric effect is positive (relative to the assumed axis direction c) at compressive stresses ($a < a_0$) and negative at tensile stresses ($a > a_0$). Therefore, at tensile stresses, the direction of polarization associated with the piezoelectric effect

GaN and AlN crystal lattice parameters

Parameter	a, Å	P_{SP}, C/m^2	e_{31}	e_{33}	C_{13}	C_{33}
GaN	3.189	−0.034	−0.17	0.29	92.0	389.9
AlN	3.112	−0.090	−0.60	1.34	101	387.6

coincides with the direction of spontaneous polarization, and at compressive stresses is opposite to spontaneous polarization. Al(Ga)N thin layer is subject to tensile stresses on a GaN thick layer.

Different values for elastic and piezoelectric parameters GaN and AlN are discussed in the literature (see, for example, [6,8,9]). The values used in this work [10,11] are given in the table ($C_{13,33}$ in GPa, $e_{31,33}$ in C/m^2).

When designing the transistor design, it is necessary to take into account the high concentration of background impurities in GaN grown using MOCVD and MBE technology. Key impurities: small donors — background silicon and oxygen, deep acceptor — carbon. It is indicated in the literature [12–14] that usually the concentration of each impurity element varies in the range $10^{16}-10^{17}\,\mathrm{cm}^{-3}$. A low total electron concentration can be achieved with compensation at the level of $5\cdot10^{16}\,\mathrm{cm}^{-3}$ [15]. It is preferable to obtain the lowest possible concentration of background impurities during the growth process. It was shown in [16] that silicon and oxygen impurities can diffuse from the substrate and concentrate on the GaN/AlN heterojunction. Being donors, they partially compensate for holes, create a large number of recombination centers and reduce the mobility of charge carriers in the channel, which leads to an increase in leakage currents and resistance of the transistor in the open state (R_{on}).

Carbon alloying is the most common method of oxygen and silicon compensation [17]. However, in this case, due to the inertia of technological processes, the presence of residual precursors in the growth chamber and diffusion, unintentional doping of the channel layer with carbon is possible. Typical carbon pollution reported using MOCVD growth technology is $\sim 10^{16}\,\mathrm{cm}^{-3}$ for growth at 78 Torr and $\sim 10^{18}\,\mathrm{cm}^{-3}$ for growth at atmospheric pressure [18].

The simulation was carried out using Sentaurus TCAD (Synopsys Inc.). Charge transfer was calculated using a drift-diffusion model. Deep impurities were accounted for using a single level described in the framework of the Shockley-Read-Hall model.

3. *p*-channel GaN/AlN transistor with Schottky barrier

Figure 1 shows the simplest design of a *p*-channel transistor manufactured using the GaN-on-Si technology. The transistor structure includes AlN thin stressed barrier layer grown on the surface of the relaxed GaN and overgrown with an unalloyed GaN top layer. The gate is a Schottky barrier and is made by applying metal to the GaN cover

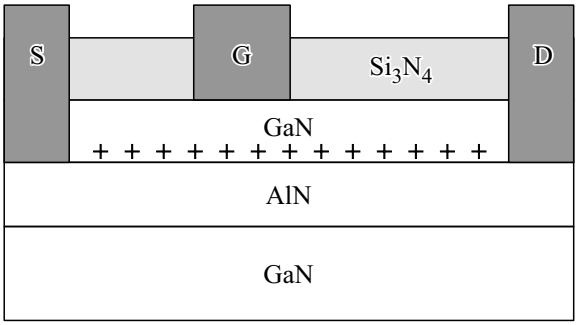

Figure 1. Design of *p*-channel Schottky gate transistor based on GaN/AlN/GaN heterostructure.

layer. The resulting polarization difference at the GaN/AlN heterointerface $(P_{SP}(\mathrm{AlN}) + P_{PE}(\mathrm{AlN}) - P_{SP}(\mathrm{GaN}))$ produces a negative surface charge. This charge generates an electric field that ionizes the electronic states in the valence band and at the heterointerface and thereby enriches the boundary region with holes. The holes are located in a triangular quantum well formed as a result of bending the edge of the valence band. The existence of a high density hole gas (2DHG) in unalloyed GaN/AlN structures was experimentally confirmed in [4].

The dependence of the concentration of two-dimensional hole gas p_s on the thicknesses of AlN stressed barrier layer (d_{AlN}) and GaN top cover layer (d_{GaN}) is shown in Figure 2. The chart shows that the concentration of holes weakly depends on thickness at the layer thicknesses of GaN > 25 nm. On the other hand, the layer concentration of holes increases from 0 to $2.5\cdot10^{13}\,\mathrm{cm}^{-2}$ as the AlN thickness increases. Such concentration values correspond to the resistance ~ 7 kOhm/square. The layer concentration of holes becomes $< 10^{11}\,\mathrm{cm}^{-2}$ and the layer resistance is equal to > 100 kOhm/square with a layer thickness of AlN < 3 nm. The layer concentration of holes can decrease and resistivity can increase with small thicknesses of the AlN barrier (< 3 nm) due to the roughness and imperfection of the heterointerface [19].

It can be seen from the chart that the thickness of the GaN layer should be > 30−40 nm for manufacturing *p*-channel transistor. On the other hand, there is a critical thickness of the AlNd_c barrier layer below which it remains stressed. The critical thickness of $d_c \approx 6.5$ nm is calculated using an approximate estimate [20] $d_c \propto b/2\delta$, where $b = 0.3189$ nm —the length of the Burgers vector in stressed AlN, and $\delta = 0.024$ — the relative deformation of AlN. If the thickness d_{AlN} is greater than d_c, relaxation of the tensile stressed AlN occurs and the deformation energy is released in the form of cracks along the hexagonal planes. This has been observed experimentally in AlN/GaN HEMT structures [21,22]. Structures with AlN layer thickness of $d_{\mathrm{AlN}} > 7$ nm showed hexagonal cracks on the surface when scanned using atomic force microscopy. These cracks lead to suppression of hole mobility and are therefore undesirable. The piezoelectric polarization $P_{PE}(\mathrm{AlN})$ decreases as

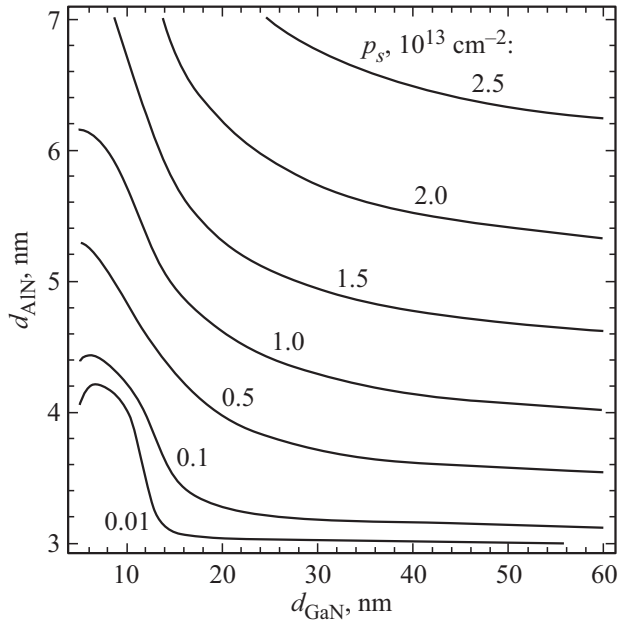

Figure 2. The dependence of the layer concentration p_s of a two-dimensional hole gas on the thicknesses of AlN stressed barrier layer (d_{AlN}) and the strongly doped GaN layer (d_{GaN}).

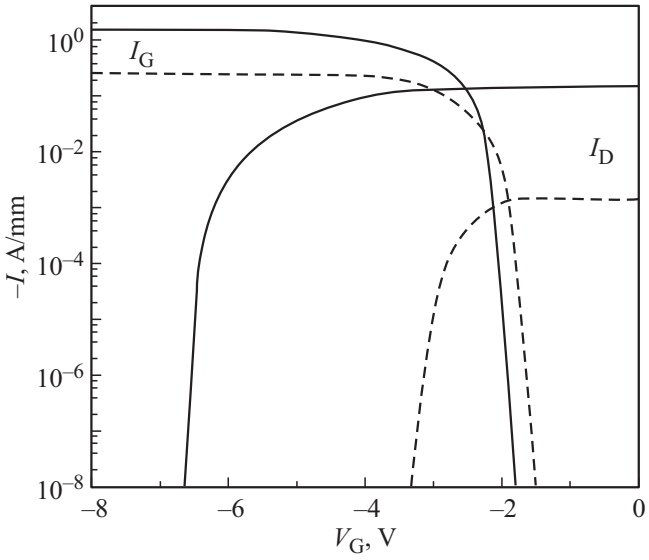

Figure 3. The dependence of the drain current (I_D) and the gate current (I_G) on the value of the gate-source voltage for transistors with AlN layer thickness of 5 nm (solid line) and 3 nm (dotted line).

a result of relaxation and the layer concentration of holes decreases as a result, as well.

Figure 3 shows the dependences of the drain current (I_D) and gate current (I_G) on the value of the gate-source voltage for transistors with AlN layer thickness of 5 nm (solid line) and 3 nm (dotted line). The drain-source voltage was considered to be equal to -15 V. The background impurities of silicon and oxygen are completely compensated by carbon. It can be seen from the chart that the threshold voltage increases with the increase of AlN thickness because the layered concentration of two-dimensional hole gas increases. The transistor can be considered closed at thicknesses of < 2.5 nm. An important feature of the transistor design under consideration is the occurrence of large leakage currents into the gate when the gate voltage is greater than the height of the Schottky barrier. The graph shows that the height of the Schottky barrier is less than the threshold voltage. Typical values of the metal work function are in the range of 4–5 eV. Therefore, the height of the barrier cannot be changed much by replacing the metal, and, as a result, it is impossible to prevent the leakage currents into the gate.

4. Insulated gate transistor

The schematic design of the transistor is shown in the box to Figure 4. The gate metal is separated from the semiconductor by a dielectric layer. Due to the high concentration of holes in the quantum well on the heterointerface, large threshold voltages are required to control the transistor. It is necessary to use materials with a large electric breakdown field as a gate insulator, for example, Al_2O_3. The threshold voltage (V_{th}) in the MOS structure is proportional to the source-to-gate ratio of charge to the respective capacitance, Q_{SG}/C_{SG}. The charge Q_{SG} can be controlled by changing the thickness (d_{GaN}) and the doping level of the GaN cover layer. With a fixed thickness of the gate insulator, the capacitance C_{SG} can be approximated by the formula of a flat capacitor and, thus, $C_{SG} \propto d_{GaN}^{-1}$. The charge Q_{SG} can be reduced by doping the GaN cover layer with a donor impurity, such as silicon, and compensating for holes in the channel for reducing the threshold voltage and obtaining a controlled MOS transistor. However, this increases the resistance of the transistor in the open state (or reduces the drain current) due to carrier scattering.

Figure 4 shows the dependence of the threshold voltage and maximum drain current on the thickness of the GaN cover layer doped with silicon to a concentration of 10^{19} cm^{-3}. The thickness of AlN barrier layer is 4 nm. Calculations showed that the sub-barrier region is completely depleted of electrons if the layer thickness is GaN < 40 nm, and the conductivity is determined only by the properties of a two-dimensional hole gas. The chart shows that the optimal thickness of n^+-GaN for manufacturing of p-channel transistor with high drain currents is 12–17 nm, approximately corresponding to the region of a two-dimensional hole gas. The maximum drain current will increase from 0.2 to 7–8 mA/mm with an increase in the thickness of the AlN barrier layer to 7 nm. However, in this case, the threshold voltage will be > 10 and a breakdown of the gate insulator is possible.

The cultivation of a highly alloyed GaN layer makes it possible to combine the manufacturing of a p-channel

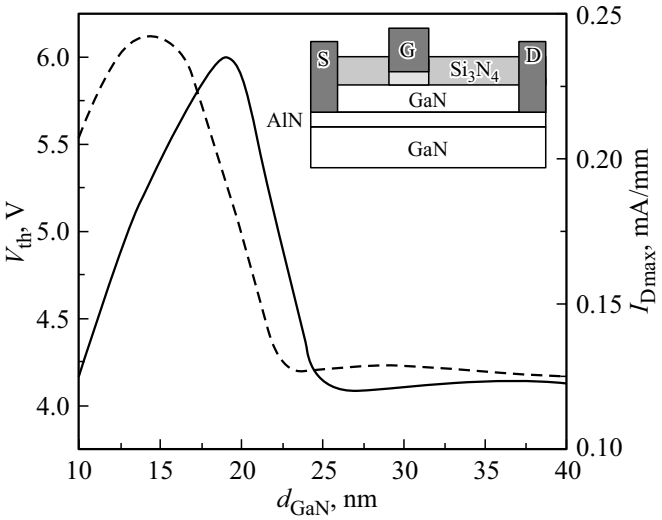

Figure 4. Dependence of the threshold voltage V_{th} (solid line) and the maximum drain current $I_{D\,max}$ (dotted line) on n^+-GaN layer thickness.

transistor with the manufacturing of non-fused ohmic contacts for a *n*-channel transistor and, producing a monolithic complementary pair of transistors in a single technological process in the future. Currents ~ 1 A/mm [23,24] are observed in *n*-channel transistors based on AlN/GaN heterostructures. $\sim 10^{-5}-10^{-3}$ A/mm currents depending on the thickness of the AlN layer will be reached in *p*-channel transistors with an isolated gate on a similar structure. The difference in transistor current levels cannot be equalized by changing only the gate width ratio. It is possible to dope the channel layer of GaN with carbon and thereby increase its resistance to reduce current misalignment. In this case, the Fermi level shifts to the edge of the valence band, the electron concentration in the two-dimensional electron gas layer decreases, and the holes in the two-dimensional hole gas layer increases.

5. Reverse gate transistor

It is necessary to manufacture a *p*-channel transistor with a current level of $\sim 0.1-1$ A/mm to take advantage of the current-matched complementary logic. Consider the design of a transistor with a gate formed by a two-dimensional electron gas from the substrate side. The diagram of the transistor structure is shown in the box to Figure 5. A through etching of the upper GaN layer and the AlN barrier layer is performed with deepening into the underlying GaN layer for the manufacturing the gate electrodes. Next, low-resistance ohmic contacts for the two-dimensional electron gas region are formed by successive deposition of layers of titanium, aluminum, nickel and gold and thermal annealing. In this case, AlN thin barrier layer performs the function of a gate insulator. Modern epitaxial technologies make it possible to grow stressed AlN layers with a low density of penetrating dislocations and thereby ensure low leakage currents into the gate.

The absence of a control electrode between the drain and the source makes it possible to effectively use the upscaling of the drain-source distance (L_{SD}) to increase the maximum drain current I_{Dmax}. Reduction of L_{SD} increases the electric field strength and reduces the voltage drop. Reduction of L_{SD} should also increase the speed of the field transistors. However, L_{SD} upscaling should take into account the breakdown voltage requirements of the transistor.

Figure 5 shows a set of dependencies of the maximum drain current density at saturation on the

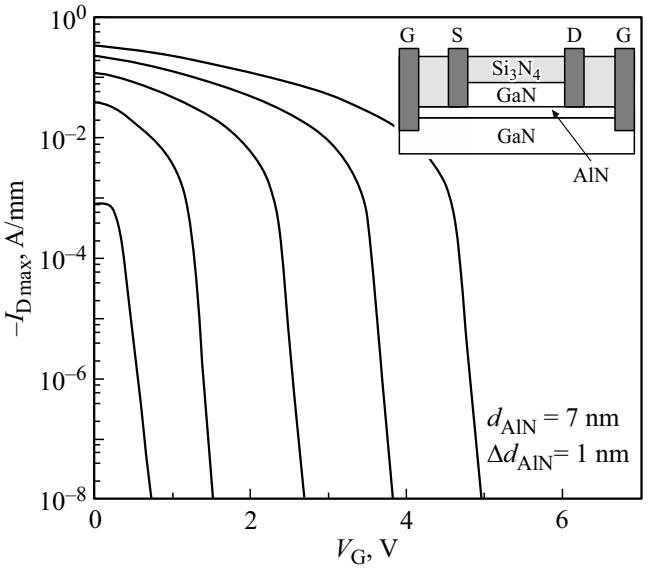

Figure 5. The dependence of the maximum drain current density at saturation on the gate voltage at different thicknesses of the AlN barrier layer in the range $d_{AlN} = 3-7$ nm.

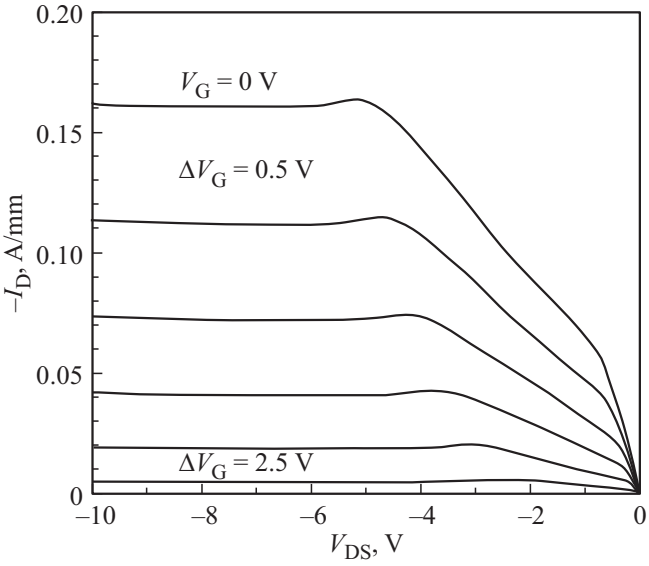

Figure 6. Output characteristics of a gate transistor in a two-dimensional electron gas layer.

gate voltage with different thicknesses of the AlN barrier layer. $L_{SD} = 4.25$ nm. In this case, the values of $I_{Dmax} > 0.1$ A/mm are observed at AlN thicknesses of > 5 nm. The design of the transistor in question makes it possible to increase the maximum current density compared to the design with an isolated gate. Typical output characteristics for a transistor with a barrier layer thickness of 5.5 nm are shown in Figure 6. Maximum transconductance is ~ 100 mS/mm. The drain current and transconductance can be increased by 1.5–2 times in case of L_{SD} upscaling depending on the available manufacturing technology. For a given threshold voltage, the AlN thickness can be selected, providing an acceptable value of resistance in the open state R_{on} and a minimum change in the characteristics of the transistor with a technological variation of the parameters of the barrier layer.

6. Conclusion

Currently, *p*-GaN/AlGaN/GaN is the closest for commercialization structure for manufacturing of a *p*-channel transistor. The disadvantage of this structure is the relatively high ionization energy of the atoms of the acceptor impurity Mg (150–200 MeV). Due to incomplete ionization of the impurity, the maximum achievable value of the volume concentration of holes does not exceed 10^{18} cm^{-3} [25]. Mg doping to a concentration of $2 \cdot 10^{19}$ cm^{-3} is usually used. Amorphization of the material occurs in case of high concentrations of impurities, the concentration of holes varies slightly [26] and the mobility significantly decreases [27]. Due to the low density and mobility of charge carriers in the channel, the drain currents of transistors do not exceed 100 mA/mm.

The reverse gate design based on the GaN/AlN/GaN heterostructure considered in this paper does not have this disadvantage. A polarizing charge is used to create a hole gas. The polarization charge is independent of the Fermi level, and therefore it does not shield the gate's electric field. It should also be noted that due to the high piezoelectric properties of AlN on the considered structure, it is possible to integrate passive radio frequency components such as filters, waveguides and antennas into a single monolithic circuit.

The second problem for these structures is ohmic contacts to the region of a two-dimensional hole gas. A Schottky barrier with a height of 1.6–2.5 eV always occurs at the metal-semiconductor interface due to the wide band gap of gallium nitride (3.4 eV) and typical values of the metal work function in the range of 4–5 eV [28]. The problem of creating ohmic contacts with a resistance of the order of several ohms · mm can be solved using epitaxial buildup of highly alloyed layers *p*-InGaN [29] or indium tin oxide (ITO) [30].

Conflict of interest

The authors declare that they have no conflict of interest.

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