Technical Physics Letters, 2024, Vol. 50, No. 4

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Tunnel diodes n^{++}-GaAs:(δ-Si)/p^{++}-$Al_{0.4}Ga_{0.6}As$:(C) for connecting elements of multijunction laser photoconverters

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Received October 24, 2023
Revised December 21, 2023
Accepted December 21, 2023

Based on mathematical modeling, there has been proposed a new type of thermally stable connecting tunnel diode with an intermediate i-layer, which is promising for implementing highly efficient multijunction laser photoconverters. Two types of the n^{++}-GaAs/p^{++}-$Al_{0.4}Ga_{0.6}As$ tunnel diode structures have been grown by molecular beam epitaxy: with and withput the intermediate i-GaAs layer. It has been experimentally demonstrated that the inclusion of a nanoscale i-layer between the n^{++}— and p^{++}-regions of the tunnel diode provides an increase in the density of peak tunneling current J_p. Due to the epitaxial wafer annealing which simulates a long-term process of epitaxial growth of multijunction laser-radiation photoconverters, the structure with the i-layer exhibited a 30-% increase in peak tunneling current J_p.

Keywords: mathematical modeling, connecting tunnel diode, i-layer, molecular beam epitaxy, multijunction laser photoconverter.

DOI: 10.61011/PJTF.2024.07.57469.19777

Due to their high output electrical power, monolithic multijunction photoconverters (MMPCs) of laser radiation are currently promising for application in various fields of science and technology, including radiophotonics [1], microelectronics [2] and medicine [3]. In the first of these areas, MMPCs are helpful in creating relatively short fiber-optic communication lines and radiophotonic phased antenna arrays [1]. The short (up to 1 km) length of such fiber-optic communication lines allows operation in the spectral range of 700−900 nm where high efficiency is possessed by the GaAs/AlGaAs photoconverters [4].

Each MMPC consists of several photoactive subelements with the same band gap and similar compositions but with different thicknesses and doping levels of the epitaxial layers. This design ensures in the MMPC photovoltaic operating mode not only efficient conversion of monochromatic radiation with a power higher than that in the case of single-junction photoconverters, but also better matching with the load. The monolithic MMPC subelements are interconnected by back-to-back nanoscale tunnel diodes (TDs). The connecting elements should possess high optical transparency, high density of peak tunnel current (J_p) exceeding the photoconverter short-circuit current, and low differential resistance necessary to minimize the voltage drop across TD. The goal of this work was research aimed at creating a new type of thermally stable connecting tunnel diodes necessary for constructing highly efficient monolithic multijunction photoconverters of laser radiation.

As the basic version of TD for the 700−900 nm MMPCs, the n^{++}-GaAs/p^{++}-AlGaAs structures are used. Peak current J_p of the forward-bias TD current-voltage characteristic (JV characteristic) is largely determined by the free charge carriers concentration in degenerate layers. However, it should be taken into account that long duration of the epitaxial growth of an MMPC structure having a characteristic thickness of several micrometers causes smearing and mutual compensation of dopant profiles and, hence, a decrease in the charge carrier concentration and degradation of the TD JV characteristic [5].

In addition, reaching in GaAs layers an electron concentration exceeding $2 \cdot 10^{19}\,\mathrm{cm}^{-3}$ by any method of introducing a donor dopant (Si, Te) is a complex technological task [6]. According to data of [6], one of the mechanisms significantly restricting the electron concentration in n-GaAs (curve *1* in Fig. 1) is gallium vacancies (V_{Ga}). When GaAs is doped with Si atoms, the donors $_{0.4}V_{Ga}$ interaction gives rise to stable complexes. Those complexes can significantly reduce the doping efficiency. The doping efficiency noticeably decreases at the donor impurity concentration $N_D > 3 \cdot 10^{18}\,\mathrm{cm}^{-3}$. Ga vacancies get compensated by donors (Si), and the free electron concentration rises as a sublinear function like $\sim N_D^{1/3}$ regardless of the dopant introduction method. The mentioned problems may be possibly solved by using dopants with low diffusion coefficients, e.g. carbon atoms as an acceptor dopant, δ-doping with donors in creating a degenerate n^{++}-GaAs region, reducing the epitaxial growth temperature, and including an intermediate undoped i-GaAs nanolayer between the degenerate n^{++}— and p^{++}-layers [7]. According to the previously performed numerical modeling of the connecting n^{++}-GaAs (10 nm)/i-GaAs (0−7 nm)/p^{++}-$Al_xGa_{1-x}As$

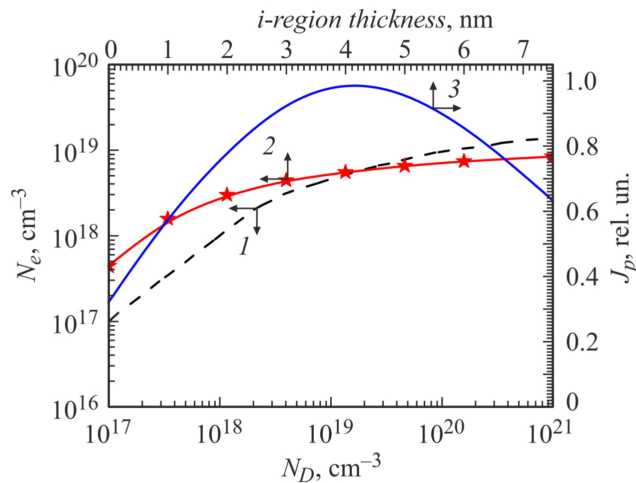

Figure 1. Calculated free electron concentration versus donor dopant concentration in n-GaAs [6] (*1*), free electron concentration in the n^{++}-GaAs degenerate region versus the thickness of the n^{++}-GaAs/i -GaAs/p^{++}- Al$_{0.2}$Ga$_{0.8}$As TD i layer [7] (*2*) and J_p values versus the thickness of the n^{++}-GaAs/i-GaAs/p^{++}-Al$_{0.2}$Ga$_{0.8}$As TD i layer [7] (*3*).

(10 nm) ($x \geqslant 0.2$) $p{-}i{-}n$ TDs, including an undoped i-nanolayer between the n— and p-type degenerate layers allows increasing J_p of the $p{-}i{-}n$ TDs. In [7], the calculated J_p dependence on the i–layer thickness was obtained (curve 3 in Fig. 1) taking into account two tunneling mechanisms (nonlocal interband quantum tunneling and tunneling through traps [8]). J_p increases with increasing thickness of the i-layer, reaches maximum at the i-layer thickness of ~ 4 nm, and then decreases due to an increase in thickness of the potential barrier the carriers tunnel through. This effect is observed mainly for TDs with heterojunctions and is associated with impacts of a number of factors. As curve *2* in Fig. 1 shows, an increase in the i-layer thickness results in a decrease in the depletion degree of the nanoscale degenerate n^{++}-GaAs layer and increase in the concentration of free electrons available for tunneling, which promotes an increase in J_p. As per the calculated band diagrams of the TD active region (see Fig. 2, a), the GaAs/Al$_x$Ga$_{1-x}$As heterobarrier gives rise to an energy jump for the conduction-band major carriers, which reduces the probability of quantum tunneling. However, inclusion of a nanoscale i-layer to a certain thickness promotes reduction in wave vector $k(x)$ integral in expression

$$\tau(E) = \exp\left(-2\int_{x_{beg}}^{x_{end}} k(x)dx\right) \qquad (1)$$

and, hence, an increase in the quantum tunneling probability [7]. In formula (1), x_{beg} and x_{end} are the start and end points of the charge carrier tunneling path through the barrier, k is the wave vector. In addition, according to [9], the effective electron mass in a thin slightly doped i-layer will be significantly lower than that in degenerate

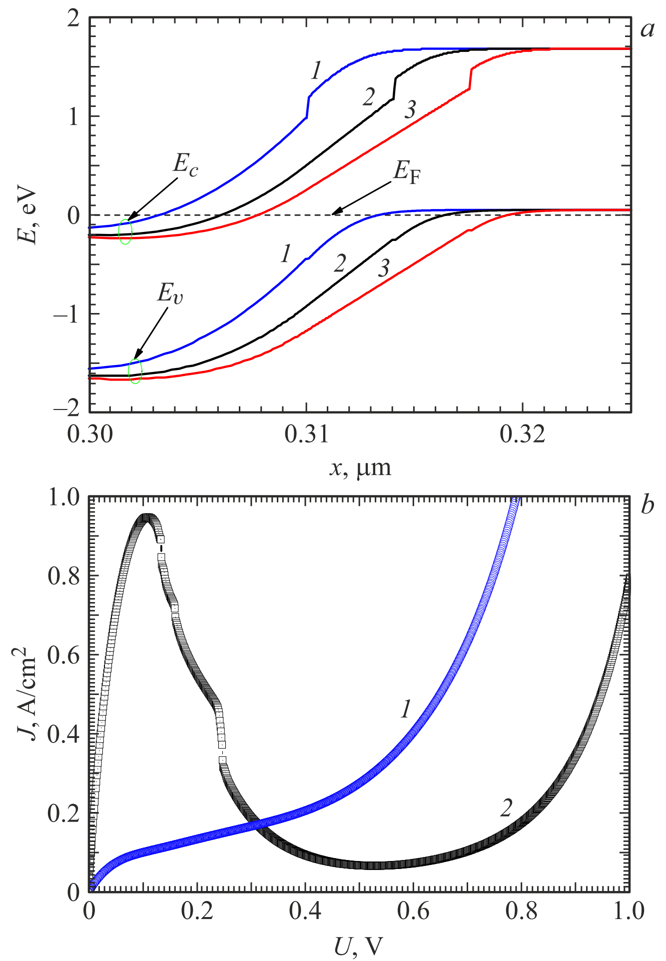

Figure 2. a — band diagrams of the n^{++}-GaAs/i-GaAs/p^{++}-Al$_{0.2}$Ga$_{0.8}$As TD [7] for the i-layer thicknesses of 0 to 7.5 nm at bias voltage $U = 0$. i-layer thicknesses, nm: *1* — 0, *2* — 4, *3* — 7.5. b — experimental direct JV characteristics of the n^{++}-GaAs:(δ-Si)/i-GaAs/p^{++}-Al$_{0.4}$Ga$_{0.6}$As:(C) TDs. *1* — structure A, *2* — structure B.

Table 1. Structure A design

Layer type	Thickness, nm	$N_{D,A}$, cm^{-3}
p^+-Al$_{0.6}$Ga$_{0.4}$As:(C)	50	$1 \cdot 10^{19}$
p^{++}-Al$_{0.4}$Ga$_{0.6}$As:(C)	10	$1 \cdot 10^{20}$
n^{++}-GaAs:(δ-Si)	10	$\geqslant 1 \cdot 10^{19}$
n^+-Al$_{0.6}$Ga$_{0.4}$As:(δ-Si)	50	$4 \cdot 10^{18}$

TD layers, which also contributes to an increase in J_p. Just the combination of these factors induces the emergence of an extremum in curve *3* (Fig. 1) at the i-layer thickness of ~ 4 nm. A further increase in the i-layer thickness leads to a decrease in the probability of quantum tunneling through the barrier and reduction in J_p.

Using molecular beam epitaxy (MBE), TD structures of two types were grown on n-type GaAs substrates (76.2 mm in diameter): A (Table 1) and B (Table 2). The structures

Table 2. Structure B design

Layer type	Thickness, nm	$N_{D,A}$, cm^{-3}
p^+-$Al_{0.6}Ga_{0.4}As$:(C)	50	$1 \cdot 10^{19}$
p^{++}-$Al_{0.4}Ga_{0.6}As$:(C)	10	$1 \cdot 10^{20}$
i-GaAs	7	$\geqslant 5 \cdot 10^{14}$
n^{++}-GaAs:(δ-Si)	10	$\geqslant 1 \cdot 10^{19}$
n^+-$Al_{0.6}Ga_{0.4}As$:(δ-Si)	50	$4 \cdot 10^{18}$

had the form of tunnel heterojunction n^{++}-GaAs/p^{++}-$Al_{0.4}Ga_{0.6}As$. The degenerate n^{++}-type GaAs layers were δ-doped with Si, while the p^{++}-$Al_{0.4}Ga_{0.6}As$ layers were doped with C atoms. Doping levels of the n^{++} and p^{++} layers in the structures were $\geqslant 1 \cdot 10^{19}$ and $\sim 1 \cdot 10^{20}$ cm^{-3}, respectively. Heavily doped regions for both structures were grown under identical conditions at the substrate temperature of $\sim 535-550$°C. As compared to structure A, structure B contained, in addition, an undoped i-GaAs layer ~ 7 nm thick. The size of the i-layer was chosen with regard to the effect of the Si dopant temperature diffusion during the subsequent growth of the MMPC structure [7]. After the epitaxial growth was completed and samples were withdrawn, individual fragments of the grown heterostructures were subjected to annealing in the MBE chamber in order to simulate the growth process of real MMPCs. On the grown structures, TD mesas $(4-8) \cdot 10^{-4}$ cm^2 in area were formed.

For structures A and B, JV characteristics of TD samples with the mesa diameter of 225 μm located at different places of the wafer were measured directly on the wafer. The JV characteristics were measured at positive bias voltage of up to 1 V and room temperature $T = 300$ K. Fig. 2, b presents the JV characteristics measured for TD with the mesa diameter of 225 μm for structures A and B under study with maximal J_p values. Notice that JV characteristic of the structure A TD is relevant, to a high extent, to a reversed diode, which may be due to a weak degeneracy level of the n^{++}-GaAs:(δ-Si) region. The JV characteristic does not exhibit a section with negative differential resistance because in the case of direct bias voltage the peak tunnel current J_p corresponding to interband quantum tunneling is comparable with the valley current density (J_v) which, according to the JV characteristics of the structure B samples, is ~ 0.1 A/ cm^2. JV characteristics of the structure A diodes contain in the voltage range of 0 to 50 mV a quasi-linear section corresponding to interband quantum tunneling with $J_p \sim 0.1$ A/cm^2.

In structure B, a JV characteristic typical of TD with interband quantum tunneling was observed due to the presence of an undoped i-GaAs nanolayer between the degenerate regions. Maximum J_p in structure B was ~ 1.0 A/cm^2. The fact that J_p values are lower than those given for the n^{++}-GaAs:(δ-Si)/p^{++}-$Al_{0.2}Ga_{0.8}As$:(Be) structures in [7] is explained by a lower doping level of the n^{++}-GaAs:(δ- Si) layer (Tables 1, 2).

Fig. 3 demonstrates the J_p values for the structure B TD samples and their positions on the wafer. Fig. 3, a corresponds to unannealed diodes, while Fig. 3, b is for diodes annealed at 580°C for 2 h in the MPE setup chamber. The annealing mode is relevant to the growth mode of subsequent photoactive layers of monolithic MMPCs. One can see that the maximum J_p for the unannealed TD of structure B is ~ 1.0 A/cm^2, while that for the annealed TD is ~ 1.5 A/cm^2. In addition, annealing stimulates an increase in the spread of J_p values for samples over the entire wafer area, which may be caused by the Si-dopant diffusion nonuniformity due to the existence of temperature gradient across the wafer during annealing.

Thus, comparison of experimental JV characteristics of the n^{++}-GaAs:(δ-Si)/p^{++}-$Al_{0.4}Ga_{0.6}As$:(C) and n^{++}-GaAs:(δ-Si)/i-GaAs/p^{++}-$Al_{0.4}Ga_{0.6}As$:(C) structures has led to the conclusion that inclusion of the i-GaAs layer ($\geqslant 5 \cdot 10^{14}$ cm^{-3}) 7 nm thick between degenerate regions n^{++}-GaAs:(δ-Si) (10 nm) and p^{++}-$Al_{0.4}Ga_{0.6}As$:(C) (10 nm) provided the presence of a tunnel characteristics even at a relatively low doping level of the n^{++}-GaAs:(δ-Si) layer. In the case of additional annealing at 580°C for 2 h which simulates the mode of growing real structures

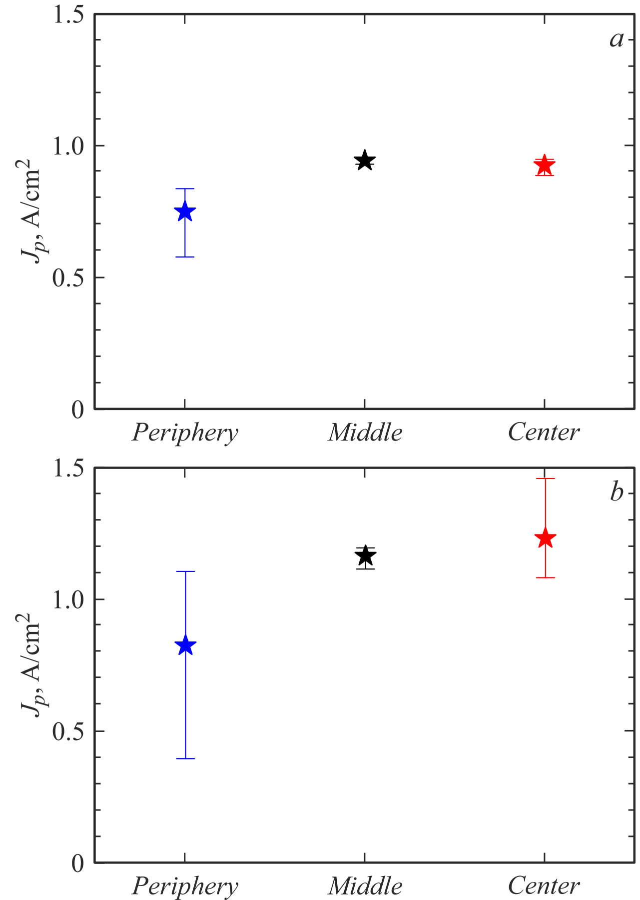

Figure 3. Peak currents J_p related to the TD sample positions (periphery, middle, center) on the structure B epitaxial wafer before (a) and after (b) annealing for 2 h at 580°C.

of monolithic MMPCs, the n^{++}-GaAs:(δ-Si)/i-GaAs/p^{++}-$Al_{0.4}Ga_{0.6}$As:(C) TD structure exhibits a 30% increase in the maximum J_p. The TD structure n^{++}-GaAs:(δ-Si)/i-GaAs/p^{++}-$Al_{0.4}Ga_{0.6}$As:(C) ensures high stability of the JV characteristics compared to those of structure n^{++}-GaAs:(δ-Si)/p^{++}-$Al_{0.2}Ga_{0.8}$As:(Be).

Conflict of interests

The authors declare that they have no conflict of interests.

References

[1] D.F. Zaytsev, V.M. Andreev, I.A. Bilenko, A.A. Berezovsky, P.Yu. Vladislavsky, Yu.B. Gurfinkel, L.I. Tsvetkova, V.S. Kalinovskii, N.M. Kontdratév, V.N. Kosolobov, V.F. Kurochkin, S.O. Slipchenko, N.V. Smirnov, B.V. Yakovlev, Radiotekhnika, **85** (4), 153 (2021). DOI: 10.18127/j00338486-202104-17 (in Russian)

[2] M. Ishigaki, S. Fafard, D.P. Masson, M.M. Wilkins, C.E. Valdivia, K. Hinzer, in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)* (IEEE, 2017), p. 2312–2316. DOI: 10.1109/APEC.2017.7931022

[3] H. Helmers, C. Armbruster, M. von Ravenstein, D. Derix, C. Schöner, IEEE Trans. Power Electron., **35**, 7904 (2020). DOI: 10.1109/TPEL.2020.2967475

[4] S. Fafard, D.P. Masson, J. Appl. Phys., **130**, 160901 (2021). DOI: 10.1063/5/0070860

[5] T. Takamoto, M. Yumaguchi, E. Ikeda, T. Agui, H. Kurita, M. Al-Jassim, J. Appl. Phys., **85**, 1481 (1999). DOI: 10.1063/1.369278

[6] W. Walukiewicz, Physica B, **302-303**, 123 (2001). DOI: 10.1016/s0921-4526(01)00417-3

[7] V.S. Kalinovskii, E.V. Kontrosh, G.V. Klimko, S.V. Ivanov, V.S. Yuferev, B.Y. Ber, D.Y. Kazantsev, V.M. Andreev, Semiconductors, **54**, 355 (2020). DOI: 10.1134/S1063782620030112.

[8] M. Baudrit, C. Algora, IEEE Trans. Electron Dev., **57**, 2564 (2010). DOI: 10.1109/TED.2010.2061771

[9] V.A. Bogdanova, N.A. Davletkildeev, N.A. Semikolenova, E.N. Sidorov, Semiconductors, **36**, 385 (2002). DOI: 10.1134/1.1469184.

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