# Research of design and technological features of manufacturing of low-noise GaAs transistors with T-gate length of 150 nm for information transmission systems

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The work presents the results of research of design and technological features of manufacturing of low-noise transistors for information transmission systems. With the software system Synopsys Technology Computer-Aided Design, the optimal parameters of heterostructure layers were determined at mole fraction of indium in the channel equal to 20%, thickness of the barrier layer 18 nm, thickness of the channel layer 12 nm and delta doping concentration $5 \cdot 10^{12}$ cm$^{-2}$. Research was conducted on the effect of the recess length of the sub-gate region of GaAs transistors on their electrical characteristics. It was found that with the increase of the recess length there is an increase in the gate-to-drain breakdown voltages of the transistor. It is revealed that additional liquid treatment before dielectric deposition decreases the specific drain current density and the transconductance of the volt-ampere characteristic, but allows increasing the gate-drain breakdown voltage of transistors.

**Keywords:** *p*HEMT, low-noise transistor, gate recess, MMIC, modeling, heterostructure.

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## 1. Introduction

Currently, the improvement of the characteristics of monolithic VHF (ultrahigh frequency) integrated circuits is largely determined by the development of technology for epitaxial growth of semiconductor heterostructures [1–8]. The quality of heterostructure growing and layers in the structure determine the limiting characteristics of VHF semiconductor devices [9–11]. It is extremely important for developing a technological process to initially select a heterostructure that ensures the best characteristics of the MMICs (microwave monolithic integrated circuits) being developed.

It is important to ensure a balance between the maximum operating drain-source voltage (gate-drain breakdown voltage) of a field-effect transistor and the specific current density of the drain for the manufacture of MMIC of low-noise amplifiers, as well as the transconductance of the current-voltage curve of the transistor. The breakdown voltage of the gate-drain increases with an increase of the length of the gate region, but at the same time the transconductance and current density of the transistor decreases. This results in a decrease of the gain and an increase of the noise figure of the transistor. In this regard, there is an optimal etching time for the recess of the gate region, which ensures the best electrical characteristics of transistors with sufficient gate-drain breakdown voltage ($\geq 9$ V).

The GaAs surface is saturated with defects and free energy levels. Free energy levels can capture charge carriers in case of exposure to the external environment, which significantly changes the shape of the input and transfer characteristics of the HEMT (high electron mobility transistor) [12–14]. Passivation of the semiconductor surface is performed after the formation of the gate for stabilization of the parameters of the transistors. SixNy is usually used as a passivating dielectric. This coating is obtained by plasma chemical deposition. The input processing before passivation allows increasing the breakdown voltage of the transistor by improving the surface quality of the heterostructure according to studies of other research teams [15–19].

The purpose of this work is to study the design and technological features of manufacturing of low-noise GaAs transistors with a T-gate gate length of 150 nm. The results obtained will be used to develop and create MMIC of low-noise amplifiers for information transmission systems.

## 2. Materials and methods

The heterostructure was simulated in the Synopsis TCAD (technology computer-aided design) software package for selection of the optimal heterostructure design that provides the required electrical characteristics of low-noise GaAs transistors in order to determine the optimal mole fraction of indium in the channel layer of $In_xGa_{1-x}As$, surface

**Table 1.** Parameters of the heterostructure layers

| Layer | Material | Thickness | Concentration of doping |
|---|---|---|---|
| Ohmic contact layer | $n^+$-GaAs | 300 Å | $5 \cdot 10^{18}$ cm$^{-3}$ |
| Stop layer | AlAs | 20 Å | *i* |
| Barrier layer | AlGaAs | 350 Å | *i* |
| $\delta$-doping | Si | – | $N$, cm$^{-2}$ |
| Separation layer | AlGaAs | 20 Å | *i* |
| Channel layer | $In_xGa_{1-x}As$ | $h_{channel}$ | *i* |
| Buffer layer | GaAs | 500 Å | *i* |
| Superlattice | AlGaAs/GaAs | – | – |
| Buffer layer | GaAs | 2000 Å | *i* |
| Substrate | GaAs (100) | 650 $\mu$m | *i* |

**Table 2.** Types of input treatments before passivation

| Number sample | Etching time recess, s | Preliminary treatment | Time, s | Additional treatment | Time, s |
|---|---|---|---|---|---|
| 1 | 60 | Isopropyl alcohol | 600 | – | – |
| 2 | | | | $HCl:H_2O$ (1:9) | 60 |
| 3 | 90 | Isopropyl alcohol | 600 | – | – |
| 4 | | | | $H_2SO_4:H_2O$ (1:9) | 60 |
| 5 | 120 | Isopropyl alcohol | 600 | – | – |
| 6 | | | | $NH_4OH:H_2O$ (1:9) | 60 |

concentration of $\delta$-doping ($N_\delta$) and the thickness of the channel layer of the transistor. The parameters of the heterostructure layers are listed in Table 1.

Two optimal heterostructure designs differing in the thickness of the barrier layer were selected based on the simulation results. These designs were grown on GaAs plates with a diameter of 4 inches. The layers were grown by molecular beam epitaxy (MBE). An experiment was conducted on these heterostructures for evaluation of the effect of the time of liquid etching of the recess of the gate region and various types of treatments before passivation on the electrical characteristics of transistor structures.

The process of manufacturing experimental samples of transistors consisted of the following blocks of technological operations. First, the mesa insulation was formed by liquid etching to a depth of 200 nm. After that, ohmic contacts with a Ni/Ge/Au/Ni/Au structure with a total thickness of 300 nm with a specific contact resistance of $\rho_k = 0.15$ Ohms/mm were formed using an electron beam evaporation unit.

A three-layer 495PMMA A4/LOR5B/495PMMA A4 mask was exposed on the electron beam lithography unit for creating a T-gate. A recess of the gate region was formed in a selective citric acid-based etcher using the liquid etching method. The time of etching of the recess of the gate area was equal to 60, 90 and 120 s. Then the metallization of the Ti/Pt/Au gate with a total thickness of 475 nm was sputtered using the electron beam evaporation unit.

The surface was passivated with $Si_xN_y$ dielectric for stabilizing the characteristics of the transistors using PECVD (plasma-enhanced chemical vapor deposition) system. The thickness of the dielectric film was 100 nm. Four types of liquid treatment listed in Table 2 were used before passivation.

The treatment in pure isopropyl alcohol (IPA) was used as a reference for comparing each of the types of input treatment before passivation with the characteristics of transistor structures at a fixed etching time of the recess of the gate region.

The dielectric was etched after passivation for opening windows for the contact pads of the source, drain and gate of *p*HEMT (pseudomorphic high electron mobility transistor). Then, the transfer characteristics of the transistors were measured on the probe station using an semiconductor device analyzer, as well as the dependence of the transconductance on the gate voltage at a voltage between the drain and the source of 1.5 V. HEMT main static parameters listed in Table 3. were calculated using these dependencies.

The optimal etching time of the gate region and the type of input processing before passivation of the semiconductor surface were selected based on the analysis of the studied parameters of the transistor. A family of current-voltage

**Table 3.** Studied parameters of transistors

| Parameter | Description |
|---|---|
| $I_{dss}$, mA/mm | Drain current per channel width unit at a gate voltage of 0 V |
| $I_{\max}$, mA/mm | Maximum drain current per channel width unit |
| $I_{d0}$, mA/mm | Leakage current across the plate surface (determined with the voltage on the gate of −2 V) |
| $G_{\max}$, mS/mm | Maximum transconductance per channel width unit |
| $V_p$, V | Transistor cut-off voltage (determined at a drain current of 1 mA/mm) |
| $V_{bd}$, V | Transistor breakdown voltage |

curves of transistors was considered for studying the operation of transistors obtained with optimal process parameters.

The shape and size of the T-gate, the depth and length of the recess of the gate region were monitored using a scanning electron microscope.

Low noise amplifier MMIC of for the $X$ frequency range were fabricated based on the GaAs $p$HEMT technological process with the best transistor parameters selected as part of the experiment.

## 3. Simulation results

The electrical characteristics of the $p$HEMT heterostructure were simulated in the Synopsis TCAD software package for determining the optimal molar fraction of indium in the channel of $In_xGa_{1-x}As$ ($x_{\text{channel}}$), the thickness of the channel layer ($h_{\text{channel}}$) and concentrations of $\delta$-doping layer ($N$). The parameters of the remaining layers of the structure are listed in Table 1.

A hydrodynamic model of current density distribution in the channel was used to calculate the HEMT electrical characteristics. The electron density is concentrated at the interface between wide-band and narrow-band semiconductors. This indicates the formation of a channel with a two-dimensional electron gas (2DEG).

Figure 1 shows the results of simulation of the transfer characteristics of a transistor depending on the concentration of $\delta$-doping with the thickness of the InGaAs channel layer $h_{\text{channel}} = 120$ Å and the molar fraction of indium in the channel $x = 0.2$.

It can be seen from the data obtained in Figure 1 that the drain current increases at a fixed gate voltage with an increase of the concentration of $\delta$-doping, but at the same time the required gate voltage increases to close the transistor. For achieving the required transistor cut-off voltage of the order of $V_p = 0.6-0.9$ V the minimum concentration of $\delta$-doping should be of the order of $N = (3-5) \cdot 10^{12}$ cm$^{-2}$.

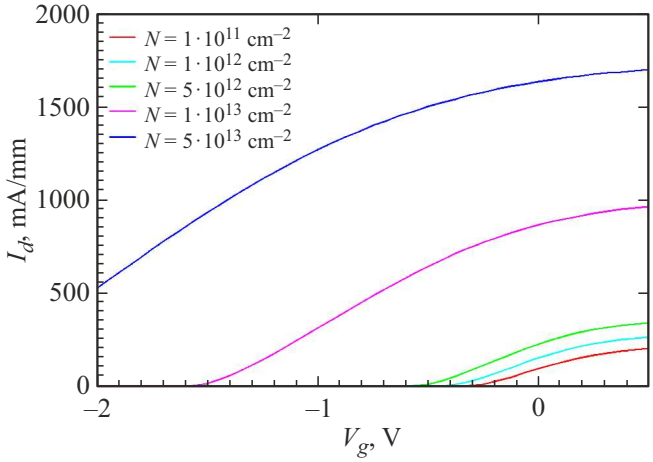


**Figure 1.** The results of simulation of the transfer characteristics of a transistor depending on the concentration of $\delta$-doping. (The color version of the drawing is provided in the electronic version of the article).

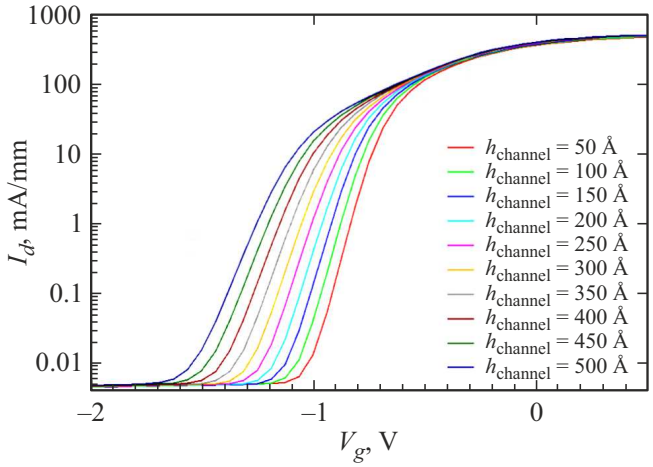


**Figure 2.** The results of calculation of the transfer characteristics of a transistor depending on the thickness of the channel layer of the transistor heterostructure.

Figure 2 shows the results of calculation of the transfer characteristics of a transistor depending on the thickness of the channel layer based on InGaAs transistor heterostructure at a concentration of $\delta$-doping of $5 \cdot 10^{12}$ cm$^{-2}$ and the molar fraction of indium in the channel of $x = 0.2$.

Figure 2 shows that the thickness of the InGaAs channel layer determines the cut-off voltage of the transistor. The thickness of the channel layer shall be within the range of $h_{\text{channel}} = 100-150$Å for achieving the required transistor cut-off voltage from 0.6 to 0.9 V. It is necessary to increase the thickness of the epitaxial layers to reduce the contribution of the error in the molecular beam epitaxy system for ensuring a high degree of reproducibility of the heterostructure characteristics from plate to plate. The thickness of the channel layer of

120 Å was chosen based on these technological recommendations.

## 4. Experimental results and analysis

The dependences of the drain current and the transconductance of the transistor per unit gate width on the gate voltage between the drain and the source equal to 1.5 V were measured using a semiconductor analyzer for various types of treatments and the etching time of the recess of the gate region. Measurements were performed for two types of structures. Figure 3, *a* and *b* show the measurement results for samples treated in pure alcohol with different etching times of the recess of the gate region. The gate width for each transistor is 100 $\mu$m.

Figure 3, *a* and *b* show that the maximum transconductance and drain current per unit width decrease of the transistor channel with an increase of the etching time of the recess of the gate region.

The HEMT static characteristics were calculated for each of the samples of transistor structures before passivation of the dielectric according to Table 3. The results of calculations of HEMT static characteristics are provided in Table 4.

The results provided in Table 4 show that the required value of the gate-drain breakdown voltage of the transistor of $> 9$ V is achieved only at an etching time of more than 90 s regardless of the type of heterostructure used.

Taking into account all the data obtained, the structure 1 has the best parameters for creating low-noise GaAs transistors and MMICs based on them with the time of etching of the recess of the gate region of 90 s and additional input treatment in $H_2SO_4:H_2O$ (1:9). The choice of the 1 structure is attributable to the fact that it ensures higher values of the maximum drain current at the corresponding value of the maximum transconductance of the transistor. Figure 4 shows the results of measurement of the family of current-voltage curves of a transistor based on the structure 1 with the time of etching of the recess of the gate region 90 s and using additional input processing in $H_2SO_4:H_2O$ (1:9). The gate voltage varied from $-2$ to 0.5 V in increments of 0.25 V.

Figure 4 shows that the maximum value of the drain current is $\sim 800$ mA/mm with a gate voltage of 0.5 V and a voltage between the drain and the source of 5 V. The transistor closes at a gate voltage between $-0.75$ and $-1.00$ V, which corresponds to the data obtained in Table 4.

The shape and size of the T-gate, the depth and length of etching of the recess of the gate region were monitored using an electron microscope. A chip was made for this purpose along a section perpendicular to the channel in the topology of the transistor structure on samples with different etching times of the gate region.

The results of the measurement of the length of the recess of the gate region at different etching times are provided in Table 5.

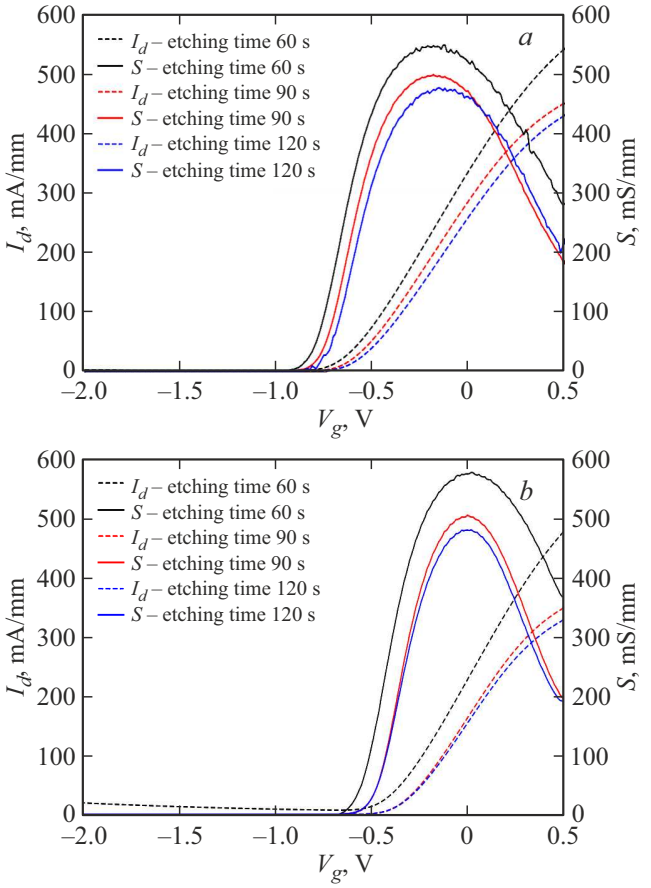


**Figure 3.** *a* — impact of the time of etching of the recess of the gate region on the HEMT transfer characteristics (structure 1). *b* — impact of the etching time of the recess of the gate region on the HEMT transfer characteristics (structure 2).

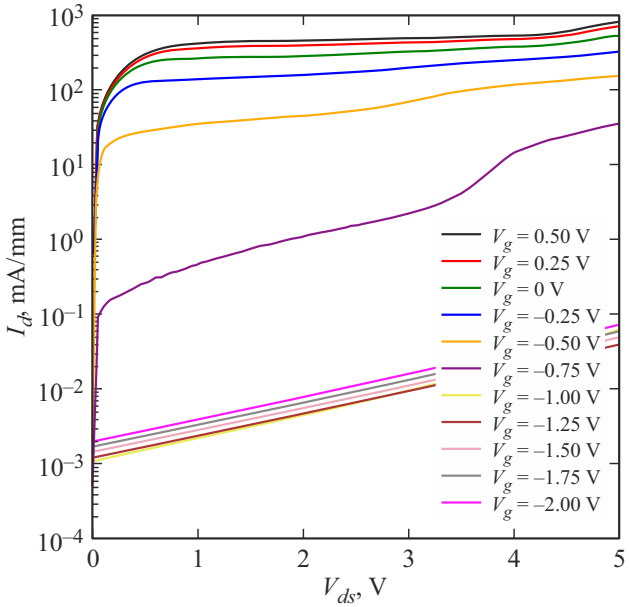


**Figure 4.** The results of measuring the family of current-voltage curves of a transistor based on the structure 1 obtained with the etching time of the recess of the gate region of 90 s and additional input treatment in $H_2SO_4:H_2O$ (1:9).

**Table 4.** Results of calculations of HEMT static characteristics

| Etching time recess, with | Type of input treatment | $I_{ds0}$, $\mu$A/mm | $I_{\max}$, mA/mm | $I_{dss}$, mA/mm | $g_{\max}$, mS/mm | $V_{S\max}$, V V | $V_p$, V | $V_{BD}$, V |
|---|---|---|---|---|---|---|---|---|
| Stricture 1 | | | | | | | | |
| 60 | IPA | 2060 | 540 | 334 | 546 | −0.20 | −0.87 | 3.0 |
| | IPA+HCl | 2680 | 534 | 324 | 544 | −0.20 | −0.95 | 5.5 |
| Variance, % | | 3,1 | −1.1 | −3.0 | −0.4 | 0 | 9.2 | 83.3 |
| 90 | IPA | 3.84 | 450 | 285 | 498 | −0.18 | −0.78 | 9.5 |
| | IPA+$H_2SO_4$ | 3.72 | 433 | 268 | 490 | −0.18 | −0.76 | 10.8 |
| Variance, % | | −3.1 | −3.8 | −6.0 | −1.6 | 0 | −2.6 | 13.7 |
| 120 | IPA | 3.10 | 430 | 258 | 476 | −0.15 | −0.75 | 11.0 |
| | IPA+$NH_4OH$ | 2.70 | 380 | 233 | 446 | −0.15 | −0.73 | 13.0 |
| Variance, % | | −12.9 | −11.6 | −9.7 | −6.3 | 0 | −2.7 | 18.2 |
| Structure 2 | | | | | | | | |
| 60 | IPA | 19300 | 476 | 227 | 576 | 0 | −0.70 | 2.5 |
| | IPA+HCl | 9730 | 461 | 208 | 575 | 0 | −0.70 | 4.5 |
| Variance, % | | −49.6 | −3.2 | −8.4 | −0.2 | – | 0 | 80.0 |
| 90 | IPA | 3.95 | 348 | 163 | 504 | 0 | −0.50 | 9.0 |
| | IPA+$H_2SO_4$ | 4.20 | 336 | 155 | 500 | 0 | −0.49 | 10.7 |
| Variance, % | | 6.3 | −3.4 | −4.9 | −0.8 | – | −2.0 | 18.9 |
| 120 | IPA | 3.01 | 328 | 154 | 479 | 0 | −0.51 | 10.5 |
| | IPA+$NH_4OH$ | 2.49 | 274 | 131 | 432 | 0 | −0.48 | 12.5 |
| Variance, % | | −17.3 | −16.5 | −14.9 | −9.8 | – | −5.9 | 19.0 |

Table 5 shows that the length of the recess increases proportionally with the increase of the etching time. The depth of etching of the recess also increases due to the limited selectivity of the etcher to the stop layer. Thus, the optimal parameters of the transistor structures were achieved with a recess length of 380 nm.

**Table 5.** The results of measurement of the length of the recess of the gate area at different etching times

| Etching time, s | 60 | 90 | 120 |
|---|---|---|---|
| Length of the recess, nm | 280 | 380 | 415 |

## 5. Development and manufacture of low-noise amplifier MMIC

MMIC of a low-noise amplifier with a frequency range from $f = 8-11$ GHz was developed and manufactured based on the selected optimal manufacturing conditions of *p*HEMT. NiCr with a specific surface resistance of 20 Ohm/square was used as a resistive material. $Si_3N_4$ with a specific capacity of 400 pF/mm$^2$ was used as the capacitor material. Conductors for interelement metallization and distributed microwave elements were fabricated on the basis of Ti/Au layers followed by electroplating of Au with a thickness of 4 $\mu$m. The reverse side of the MMIC is

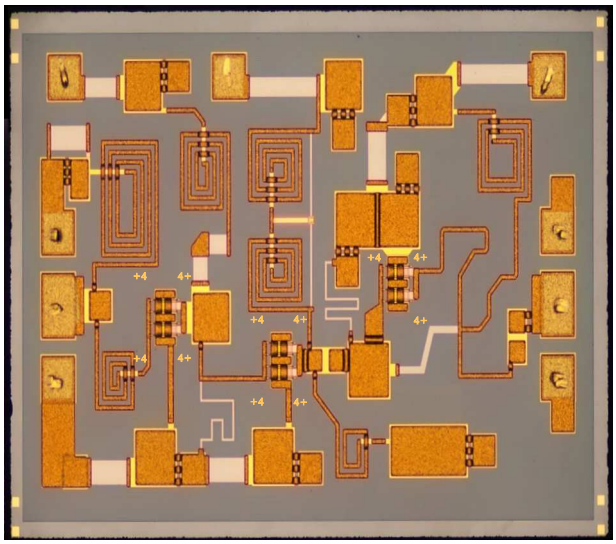

**Figure 5.** Chip view of a low-noise amplifier MMIC.

**Table 6.** The main electrical and microwave characteristics of the manufactured low-noise amplifier

| Parameter | Value | Unit of measurements |
|---|---|---|
| Frequency range | 8–11 | GHz |
| Small-signal gain | 27 | dB |
| Return losses on input | −12 | dB |
| Return losses on output | −10 | dB |
| Noise figure | 1.6 | dB |
| Supply voltage | 5 | V |
| Input current | 50 | mA |
| Cip size | $1.7 \times 1.1$ | $mm^2$ |

completely metallized with gold with a thickness of $4\,\mu$m. Figure 5 shows a chip view of the fabricated MMIC of the low-noise amplifier.

The overall dimensions of the MMIC chip of a low-noise amplifier are $1.7 \times 1.1$ mm. The VHF parameters and noise characteristics of the amplifier were studied using a vector circuit analyzer.

Table 6 shows the main characteristics of a MMIC of a low-noise amplifier.

The average gain in this range was 27 dB. The maximum value of the noise figure is 1.6 dB, which is a fairly good parameter [20].

## 6. Conclusion

The design and technology of the manufacture of low-noise GaAs transistors with a T-gate length of 150 nm were studied within the scope of this project.

Optimal characteristics of the heterostructure were selected using simulations in the Synopsys TCAD software package: the molar fraction of indium in the channel of $In_xGa_{1-x}As$, the thickness of the barrier and channel layers of the heterostructure, the concentration of $\delta$-doping of the AlGaAs barrier layer.

It was found as part of the study of the effect of the length of recess of the gate region on the HEMT characteristics that the breakdown voltages of transistors increase with an increase of the recess length because of an increase of the electrical path between the gate and the drain. Additional treatment degrades the electrical characteristics, but allows increasing the breakdown voltage of the transistors by 20%. The best characteristics according to the results of measurements of static parameters were obtained by using additional treatment in $H_2SO_4 : H_2O$ (1 : 9) after pretreatment in isopropyl alcohol with the time of etching of the recess of the gate region of 90 s (recess length 380 nm).

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### Conflict of interest

The authors declare that they have no conflict of interest.

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