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Features of the amplitude of random telegraph noise in the 2D MoS_2-based MOSFET

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Received March 26, 2024
Revised April 30, 2024
Accepted May 9, 2024

In this study there was constructed a model of the dependence of the random telegraphic noise (RTN) amplitude on the gate voltage and position of a single oxide trapped charge along the channel of MOSFET based on two-dimensional molybdenum disulfide. The RTN amplitude increases at gate voltages below the threshold one, and its dependence on the single charge position exhibits a maximum shifted from the channel center. This behavior of the RTN amplitude is explained, along with its dependence on the gate voltage, by its significant dependence on the drain voltage as well.

Keywords: two dimensional molybdenum disulfide, random telegraph noise, MOSFET, single oxide trapped charge.

DOI: 10.61011/TPL.2024.09.59145.19931

One of the trends in developing nanoelectronics is scaling of metal-oxide-semiconductor insulated gate field-effect transistors (MOSFETs) in order to minimize power consumption and enhance integration into integrated circuits. The opinion of the global scientific community regarding this trend has been recently divided into two directions. In the first direction, reduction in the MOSFET linear dimensions to 5−10 nm is assumed to be a physical limit [1], while in the second one it is believed that the size reduction may be continued by modifying the transistor structure or by using new materials for the transistor channel [2].

In the framework of the second option, one of the proposed ways of enabling further scaling is using 2D materials as a channel. One of 2D materials most frequently considered in this regard are transition metal dichalcogenides [3,4]. In particular, MOSFETs based on 2D molybdenum disulfide (MoS_2) have already been experimentally obtained [5]. Monolayers of transition metal dichalcogenides have semiconductor properties and do not possess broken bonds in the direction perpendicular to the monolayer plane [6]. This is one of the advantages of 2D materials used as a MOSFET channel as compared to the most commonly used silicon, since in this case the probability of boundary states generation is minimal. However, in the gate dielectric layers there may be observed states caused by oxide defects, which are able to capture charge carriers, single charges among them. Those single charges can initiate generation of random telegraph noise (RTN) in the MOSFET drain currents [7]. There are still no systematic studies of RTN in MOSFETs based on 2D materials, regardless of that this phenomenon seems to be very important in operation of field effect transistors. Therefore, in this work there was simulated the RTN amplitude dependence on the gate voltage and position of the single oxide trapped charge for MOSFET based on 2D MoS_2. The main task was to consider not the dynamics of RTN, but that of the stationary state after capturing a single charge in a single oxide trap.

3D modeling was performed using the TCAD Sentaurus code (Version O-2018.06, June 2018). In modeling, such tools as the Sentaurus Structure Editor (to design the transistor structure) and Sentaurus device (for modeling) were used. The MOSFET architecture was assumed to be junctionless. The transistor parameters are listed in Table 1.

Since the TCAD Sentaurus database does not include parameters of 2D MoS_2, the technique proposed in [8] was used in modeling. According to this technique, the main parameters of 2D MoS_2 were determined from experimental data and theoretical estimates and were used in modeling characteristics of MOSFET based on this material. Parameters used in modeling are given in Table 2. Simulation parameter β is adjustable and is used in the carrier mobility dependence on field strength.

In modeling, parameters of the material band structure, mobility dependence on the doping level, and achieving saturation at high fields were taken into account. The model used was calibrated by comparing the transfer characteristics obtained at the above-mentioned simulation parameters with both the simulation results given in [8] and experimental results from [5]. The comparison demonstrated a sufficiently good agreement (Fig. 1). In comparing, the model geometric dimensions and materials were the same as those of compared transistors presented in [5] and [8].

The threshold voltage was determined via the well-known formula applicable for nanoscale transistors: $I_{th} = (W_g/L_g) \cdot 10^{-7}$ A, where I_{th} is the drain current corresponding to the threshold voltage, W_g and L_g are the gate width and length, respectively. Knowing this

Table 1. Transistor parameters

Channel material	Channel thickness, nm	Channel doping level, cm^{-3}	Gate SiO_2 oxide layer, nm	Channel width, nm	Gate thickness thickness , nm	VOH Layer thickness, nm
MoS_2	0.65	10^{19}	20	160	5	54

Table 2. Simulation parameters

Charge carrier mobility, $cm^2/(V \cdot s)$	Carrier saturation rate, cm/s	Simulation parameter β	Channel material bandgap width width, eV	Electron effective electron in the channel, m0	Relative dielectric permeability of the channel
150	$1.075 \cdot 10^7$	1.6	1.8	0.463	3

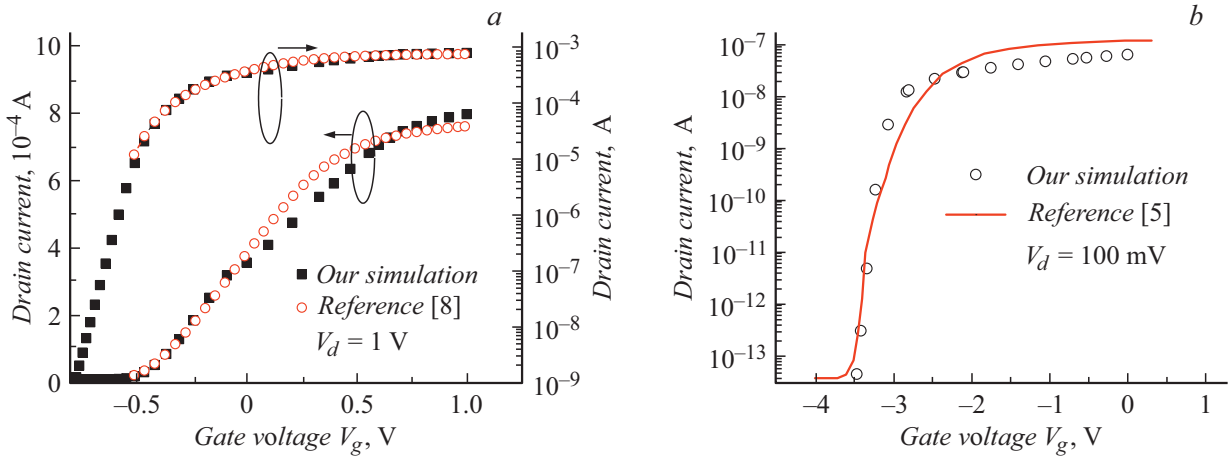

Figure 1. Comparison of the transfer characteristic of the model 2D MoS_2 based MOSFET with simulation results from (*a*) and experimental results from (*b*).

current, one can find threshold voltage V_{th} from the transfer characteristic. RTN amplitude was determined as relative variation in the drain current amplitude upon introducing the single charge. A single oxide trapped charge was simulated, according to the procedure proposed in [9], by a uniformly charged cubic region. In this work, we considered four shapes of a single oxide trap and showed that RTN amplitude is almost fully independent of the trap shape. Since the structure of the transistor under consideration is planar, the most convenient (cubic) shape of the trap has been selected from those presented in this work. Linear size of the charged region capturing the single charge is assumed to be 0.5 nm. Based on the above-presented models and simulation parameters, there were obtained the RTN amplitude dependences on the gate voltage at various single charge positions L relative to the gate edge on the side of the source along the channel middle line (Fig. 2, *a*). The results show that a noticeable increase in the RTN amplitude takes place at voltages below the threshold just as in bulk channel transistors. This is obviously caused by a more noticeable single charge effect on the drain current at its low values. The RTN amplitudes are comparable to those observed in silicon transistors with almost the same parameters [7].

The RTN amplitude dependence on the single oxide-trapped charge position L relative to the source along the channel middle line was also obtained. The simulation results show that, similarly to the case of bulk-channel MOSFET, the RTN amplitude is higher when the single charge positions are closer to the channel middle line (Fig. 2, *b*). However, here are some peculiar features. For instance, despite the potential distribution along the channel is almost uniform with a small maximum in the center (inset in Fig. 2, *b*), the RTN amplitude dependence on the single-charge position exhibits a certain shift of the RTN amplitude maximum from the channel center towards the source.

In addition, the figure shows that RTN amplitude depends also on the drain voltage. The results of modeling the RTN amplitude dependence on the drain voltage are presented in Fig. 3 for various single charge positions. Obviously,

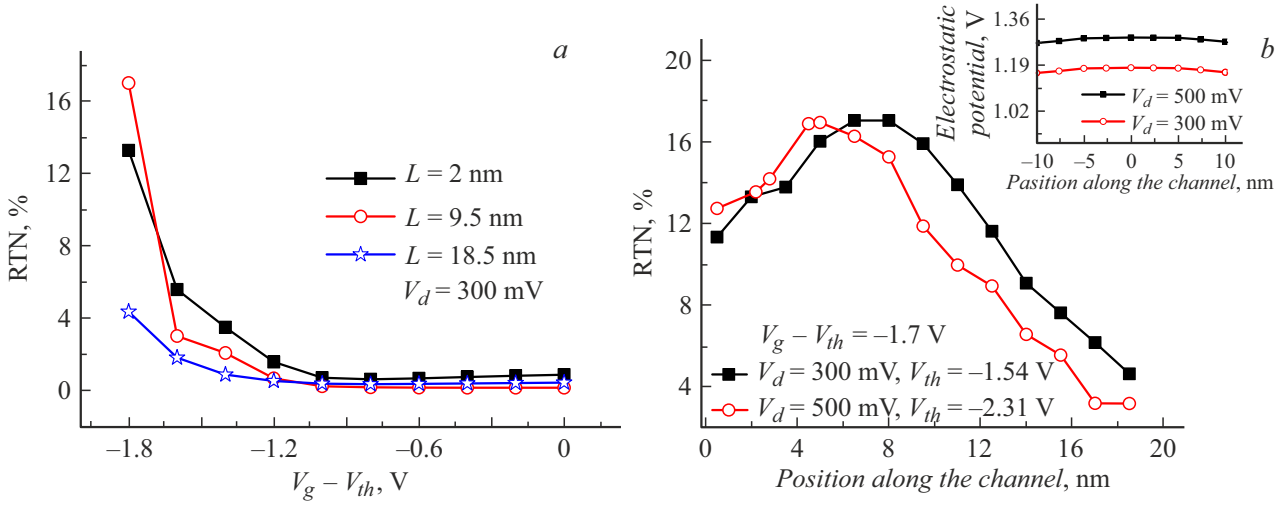

Figure 2. The RTN amplitude dependence on the difference between gate voltage V_g and threshold voltage V_{th} at different single charge positions L along the channel (a) and on the single charge position along the channel (b).

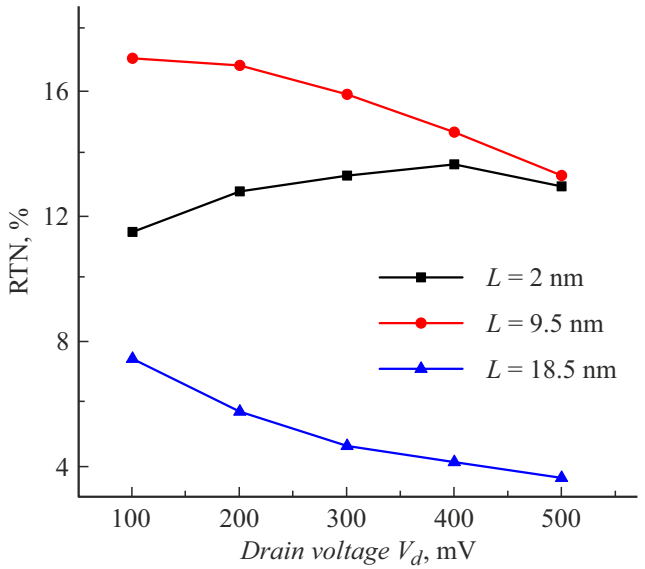

Figure 3. RTN amplitude versus drain voltage at different single charge positions L along the channel. $V_g - V_{th} = -1.7$ V.

the shift of maximum and amplitude dependence on the drain voltage, along with the single charge field effect, are associated also with the influence on the drain current of the field directed along the channel between the source and drain; this effect is caused by the source drain potential difference.

Thus, the simulation results allowed concluding that the RTN amplitude dependence on the gate voltage in a MOSFET based on 2D MoS_2 has the same character as in transistors based on bulk semiconductors. However, the distribution maximum in the RTN amplitude dependence on the single oxide trapped charge position along the channel in 2D MOSFETs is shifted from the center (in contrast to the case of bulk transistors), which is obviously caused by that the RTN amplitude depends also on drain voltage. Thus, it is obvious that in designing it is necessary to account for what the operating voltage at the designed transistor drain will be. The choice of such an operating drain voltage that will reduce the RTN amplitude depends on the single charge localization along the channel. If the single charge is localized either in the near-drain region, which can occur due to the effect of hot carrier injection, or near the center, which can take place at high operating gate voltages, the drain voltage should be best chosen relatively high. When the charge is localized near the source, the RTN amplitude depends on the drain voltage relatively weakly. In addition, Fig. 2, *a* shows that a significantly high RTN amplitude manifests itself in the subthreshold region; therefore, it would be reasonable to take into account this fact in designing subthreshold logic circuits.

Conflict of interests

The author declares that he has no conflict of interests.

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