The influence of external parameters on the switching process by delayed ionization in a silicon p^+-n-n^+-structure

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The new developed technique allows measuring fast-switching processes in semiconductor diodes, which are switched into a conducting state by applying a high-voltage fast-rising pulse together with a high DC voltage. Using this technique, delayed impact ionization was studied in structures with *n*-base thicknesses of about 100 μm and 410 μm. It has been experimentally demonstrated that for structures with a thick base, the switching characteristics improve with an increase in both the DC reverse bias and the rise rate of the applied voltage pulse. A voltage rise rate of 42.7 kV/ns has been achieved for a single structure.

Keywords: Silicon Avalanche Shaper (SAS), delayed impact ionization, sub-nanosecond voltage pulses, power diodes.

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1. Introduction

Generators of high-voltage (from a few kilovolts upward) pulses of nanosecond and sub-nanosecond duration, with repetition rates ranging from hundreds of hertz to several megahertz, which are characterized by high efficiency, long operation lifetime, compact design, and low jitter are required in a number of fields of science and technology, such as ultra-wideband (UWB) radar and communication systems [1,2], plasma-chemical technologies involving the use of cold plasma (e. g., reforming [3–5]), biological research [6–8], and plasma-assisted ignition and combustion [9–12]. Semiconductor components are the only ones that may satisfy all these requirements simultaneously.

Two-electrode silicon-based semiconductor devices utilizing delayed impact ionization are among the fastest closing-type switches [13–15]. They may assume two states: blocking (high resistance) and conducting (low resistance). The time of switching between these states lies in the sub-nanosecond range. In a high resistance state, these devices block high voltages (kilovolt-level or higher); in a low resistance, they should admit pulse currents of tens and hundreds of amperes. Diode structures of the p^+-n-n^+-type (silicon avalanche shapers, *SAS*) have been studied numerous times both experimentally and theoretically [16–19], but a detailed physical model of delayed impact ionization has not been published yet. Additional uncertainty in the analysis of operation of this class of devices is introduced by the possible spatial and temporal instabilities of various types. A limited range of variation of external parameters, which did not provide an overall pattern of operation and did not allow one to construct a reliable physical model of the mechanism under investigation, was examined in experimental studies [20–25]. The technical difficulty of accurate measurement of high pulse voltages and currents within the required time range at a high DC bias voltage also imposes certain limitations. In the present study, we propose a novel technique for measuring fast switching processes that provides an opportunity to overcome these limitations.

2. Novel method for measurement of fast switching processes

The test bench discussed in [1,2,21–25] is typically used to conduct experiments on fast processes in semiconductors, such as a sharp current cutoff in drift-step-recovery diodes (DSRDs) as a result of accumulation and extraction of electron-hole plasma at high current densities or impact ionization phenomena. These experiments necessarily involve the following stages:

1) forming of a proper voltage pulse U_g;
2) application of the formed pulse to a sample;
3) measurement of the voltage pulses at the sample and the current flowing through it.

A formed voltage pulse is fed to a sample connected in series with load, which is a set of high-voltage coaxial attenuators with an input impedance of 50 Ω. Thus, the current through the sample is $I = U_{\text{load}}/50\,\Omega$. Input pulse U_g from a generator is recorded by a frequency-compensated resistive divider, and the voltage across the sample is $U = U_g - U_{\text{load}}$.

However, the practical range of application of this circuit at high currents (hundreds of amperes) and voltages (kilo-

volts) and the required high temporal resolutions (tens of picoseconds) is rather limited. High currents, voltages, and powers necessitate an increase in the size of components of the test bench (including the resistive divider for measuring the shape of the voltage signal applied to the sample), which leads to an enhancement of parasitic parameters and has a negative effect on the temporal resolution. In addition, comprehensive studies require the application of a high DC bias voltage to the sample, and this cannot be done without the introduction of additional elements into the circuit, which also have parasitic parameters.

In view of the above, we decided to develop a new approach instead of trying to modify the existing experimental procedure. The key factors taken into account in the design of a new broadband test bench, which is free from the shortcomings mentioned above, are listed below:

1) Correct measurements may be carried out only when a TEM (transverse electromagnetic) wave with a transverse electromagnetic field configuration is supported in the test pathway. A TEM wave has no dispersion and provides the lowest pulse shape distortion. Waveguides of appropriate configurations should be chosen to attenuate higher (non-TEM) types of waves;

2) Parasitic modes arising at inhomogeneities (abrupt changes in geometry) of the waveguide may introduce additional error. Their influence may be represented by of equivalent parasitic capacitances and inductances. To suppress this influence, all elements of the measurement circuit should be matched with the waveguide and ensure the low distortion of shape of the primary TEM configuration of the electric field;

3) One should aim at reducing the size of elements of the measurement circuit, but their minimum dimensions are limited by the need to ensure a sufficient level of electrical strength for testing at high DC and pulse voltages;

4) Transmission lines with a wave impedance of $\rho = 50\,\Omega$ are optimal with regard to standards adopted for measurement equipment, high-frequency losses, and the transmitted power level. Therefore, all other elements of the high-frequency circuit are designed to match with such transmission lines.

Figure 1 presents the equivalent circuit of a test bench for studying the switching process with delayed impact ionization in high-voltage structures. This setup allows one to measure the current and voltage across the structure without a shunt and resistive dividers, making it possible to apply high voltages (both pulse and DC ones of several kilovolts) to the structure while suppressing higher modes. The measurement setup consists of a high-voltage pulse generator, two coaxial cables T_1 and T_3 with a wave impedance of $\rho = 50\,\Omega$, and microstrip line T_2 with a wave impedance of $\rho = 50\,\Omega$. A set of high-voltage attenuators produced by Barth Electronics, Inc. with a bandwidth of 18 GHz is used as a load. The high-voltage pulse generator is constructed based on DSRDs and has the capacity to produce voltage pulses with an amplitude of $1-4$ kV, a pulse width (FWHM) of 1.6 ns, and a rise time of 600 ps. Coaxial cable T_1 is 150 cm in length, which corresponds to a wave travel time in one direction of ~ 7.5 ns. Cable T_3 is 20 cm in length and connected to cable T_1 via matched 7-cm-long strip line T_2. The examined sample is installed into a gap in this line. Coaxial cable T_1 is sufficiently long to separate in time the initial pulse formed by the generator from the subsequent reflected pulse, which is first reflected from the sample, propagates along cable T_1 in the reverse direction to the generator, is reflected from the generator once again, and is applied to the sample for the second time 15 ns later.

Within this 15-ns-long interval, the actual circuit of the pulse feeding from the generator to the load through the coaxial cable can be replaced by an equivalent circuit consisting of an ideal generator of double amplitude with a zero internal resistance that is connected to the sample via a 50 Ω resistor (Figures 1, *b* and *d*).

The measurement procedure involves two stages. At the first stage, a calibration pulse is recorded: the examined structure is removed; the strip line gap is shorted; and a voltage pulse is supplied from the generator (see the diagram in Figure 1, *a*), recorded at the load, and stored in memory. The test bench may be presented within time interval $2T_1/c$ by the equivalent circuit in Figure 1, *b*. At the second stage, the sample under study is introduced into the gap in the strip line (see Figure 1, *c* and the corresponding equivalent circuit in Figure 1, *d*). At the initial time, the diode is in a blocking high-resistance state, and the reverse-biased $p-n$ junction is equivalent to a capacitance that is small in magnitude and depends on the applied voltage. The amplitude of the pulse applied to the diode may be twice as large as the amplitude of the initial pulse from the generator. As a result of delayed impact ionization, the diode then switches to a conducting state, current starts to flow in the circuit, voltage U_c at the cathode of the diode decreases, and, in accordance with Figure 1, *d*, assumes a value equal to the difference between doubled generator voltage U_g and the voltage drop across the equivalent resistance of cable T_1: $U_c = 2U_g - IR_{T1}$ (Figure 1, *d*). Since the impedances of cable T_1 and the load are equal (as are the currents flowing through them), the voltage drop across the impedance of cable T_1 is equal to the voltage drop across the load: $IR_{T1} = IR_{\text{load}} = U_{\text{load}}$; therefore, $U_c = 2U_g - U_{\text{load}}$. The anode voltage is equal to the load voltage ($U_a = U_{\text{load}}$), and the voltage drop across the sample is then $U_c - U_a = 2U_g - U_{\text{load}} - U_{\text{load}} = 2(U_g - U_{\text{load}})$. To enable the application of a constant bias to the sample, high-voltage blocking capacitor C and DC voltage source U_{dc} with high-resistance limiting resistor R are added to the measurement circuit (Figure 1, *c*). The capacitance of capacitor C is 470 pF, which yields a time constant of $\tau = RC = 50 \cdot 470 \cdot 10^{-12} \approx 23 \cdot 10^{-9}$ (*c*) = 23 ns at a load impedance of 50 Ω; this time interval is much longer than the generator pulse duration. Thus, the generator pulse is fed to the structure without any significant distortion. Since capacitor C is located on the opposite end from the sample of coaxial cable T_1, it does not excite any parasitic

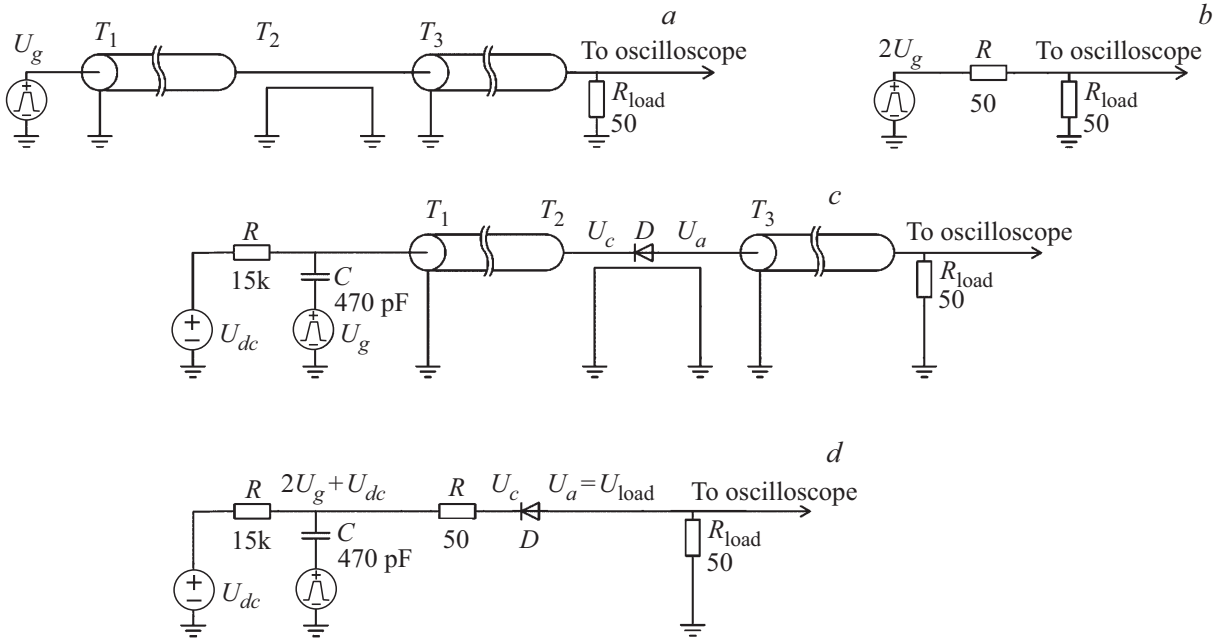

Figure 1. Test setup for the examination of high-voltage structures switching by delayed impact ionization: actual (a) and equivalent (b) circuits for recording a calibration pulse; actual (c) and equivalent (d) circuits for measuring a load voltage pulse produced by diode D.

higher modes in the measurement circuit near the sample. Thus, the voltage across the structure with a DC reverse bias is equal to

$$U_{SAS} = 2(U_g - U_{\text{load}}) + U_{dc}. \quad (1)$$

The parameters of switching under delayed impact ionization were examined experimentally in two regimes: (1) a voltage pulse with fixed amplitude U_g was applied to the sample from the high-voltage pulse generator, while DC bias U_{dc} from the voltage source was adjusted within the 0–2500 V range; (2) DC bias U_{dc} was applied to the sample from the voltage source, and a series of experiments were carried out with voltage pulses of different amplitudes U_g from the high-voltage pulse generator.

The calibration oscillograms obtained at the first stage and oscillograms of voltage pulses at the load with the sample installed in the strip line gap were then used to calculate the oscilloscope pattern of voltage across the structure under study. The current passing through the structure is equal to load voltage U_{load} divided by the load resistance of 50 Ω. Thus, if the oscillograms of current and voltage are available, then it is possible to determine the switching process duration, maximum voltage rise rate dU/dt, switching current I, maximum voltage drop ΔU across the structure at the moment of switching, residual voltage U_m, losses in the structure, and the overall efficiency of switching. The optimal operating regimes of the diode structure ensuring the most efficient generation of voltage pulses at the load can be identified through the analysis of these data. The obtained detailed information on the specifics of switching with delayed impact ionization also opens up opportunities for further optimization of the semiconductor structure aimed at improving the switching parameters or designing new devices tailored to specific engineering problems.

3. Results and discussion

The suggested novel measurement technique was tested on diode structures of a well-known, proven design and established fabrication technology that were used widely in earlier studies of delayed ionization processes [13,22,25]. The thickness of the n-type base region of these structures is on the order of $W_B = 100\,\mu$m at donor concentration $N_D \approx 1.7 \cdot 10^{14}\,\text{cm}^{-3}$. The structure area is $S \approx 1\,\text{mm}^2$. The method for measuring the voltage across the structure with a frequency-compensated resistive divider, which was used in earlier studies, did not allow for a wide range of variation of the applied DC bias voltage. Since a DC bias may exert a very strong influence on switching, special attention was paid to it in our experiments. Figure 2 presents the voltage pulses U_{SAS} on the structure, the oscillogram of the voltage pulses applied to the structure $2U_g + U_{dc}$, and current $I_{R\text{load}}$ flowing through the structure at fixed voltage pulse amplitude U_g and two different DC bias voltages $U_{dc} = 50$ V and 980 V.

Figure 3 shows the measured values of maximum switching rate dU/dt of the structure, maximum voltage drop ΔU across the structure during switching, and residual voltage U_m at the structure at pulse amplitude $U_g = 930$ V and various DC bias voltages $U_{dc} = 0$–980 V.

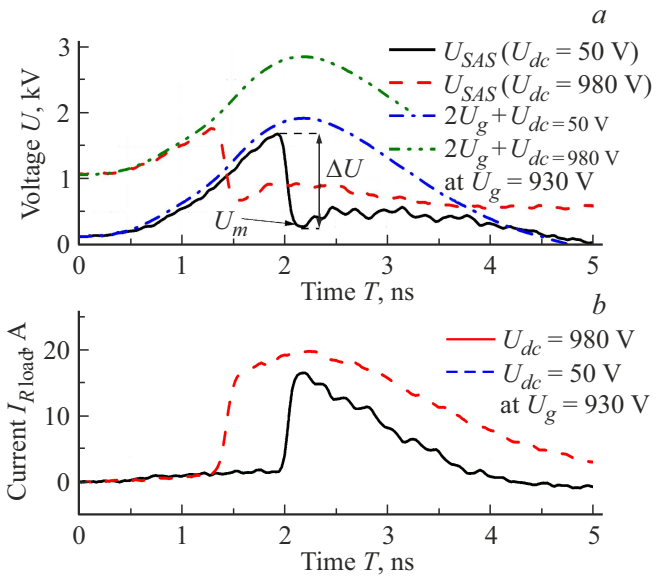

Figure 2. Oscillograms of voltage pulses U_{SAS} on the structure, applied voltage pulses $2U_g + U_{dc}$, and current I_{Rload} flowing through the structure at fixed pulse amplitude $U_g = 930$ V and two different bias voltages $U_{dc} = 50$ V and 980 V.

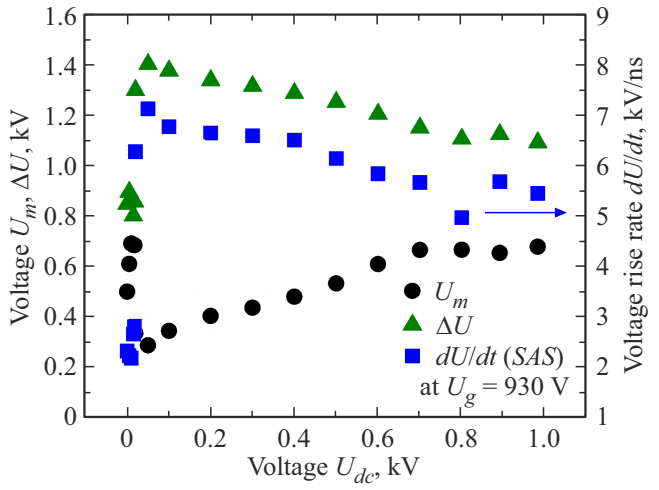

Figure 3. Dependences of switching rate dU/dt, voltage drop ΔU, and residual voltage U_m at different bias voltages U_{dc} and a fixed amplitude of voltage pulse $U_g = 930$ V from the generator.

It is evident from the data in Figure 3 that the best parameters of switching due to delayed impact ionization (specifically, the highest switching rate $dU/dt \approx 7$ kV/ns, the highest voltage drop $\Delta U \approx 1400$ V across the structure, and the lowest residual voltage $U_m \approx 300$ V) are achieved with an applied DC bias of 50–100 V. If the bias voltage drops below this optimal range or assumes higher values, the specified parameters deteriorate. It should be noted that while the improvement of switching parameters with an initial bias voltage increase within 0–50 V appears logical, the deterioration of these parameters with a further bias increase to > 100 V cannot be explained by existing models of the switching process upon delayed impact ionization and requires an additional study.

Since bias voltage $U_{dc} = 50$ V is the optimal one, it was decided to measure the dependence of switching parameters on amplitude U_g of the applied voltage pulse at this exact DC bias. Figure 4 presents the oscillograms of voltage pulses U_{SAS} on the structure, voltage pulses $2U_g + U_{dc}$ applied to the structure, and current I_{Rload} flowing through the structure at fixed DC bias $U_{dc} = 50$ V and different voltage pulse amplitudes U_g. These data agree fairly well with the results of earlier experiments performed in a measurement setup with a resistive divider [25].

Figure 5 shows the dependences of the switching rate dU/dt of the structure, the voltage drop ΔU across the structure, and the residual voltage U_m at the structure on the applied voltage pulse amplitude at DC bias $U_{dc} = 50$ V. The amplitude of pulse U_g varied within the range of 930–1900 V. It can be seen from Figure 5 that residual voltage U_m varied insignificantly, while switching rate dU/dt and voltage drop ΔU across the structure increased with increasing amplitude of the pulse from the high-voltage generator, which is unsurprising and in line with the general understanding of the switching process by delayed impact ionization.

Let us now consider a series of experiments with higher breakdown voltage *SAS* structures. These p^+–n–n^+ diode structures were fabricated via boron and phosphorus diffusion to an approximate depth of 70–80 μm and 10–15 μm, respectively, into an *n*-type silicon wafer with thickness $W = 500\,\mu$m and donor concentration $N_D \approx 1.7 \cdot 10^{13}$ cm^{-3}. The surface impurity concentration was $N_B = 5 \cdot 10^{18}$ cm^{-3} for boron and $N_P = 2 \cdot 10^{19}$ cm^{-3} for phosphorus. A positive bevel was used to protect the

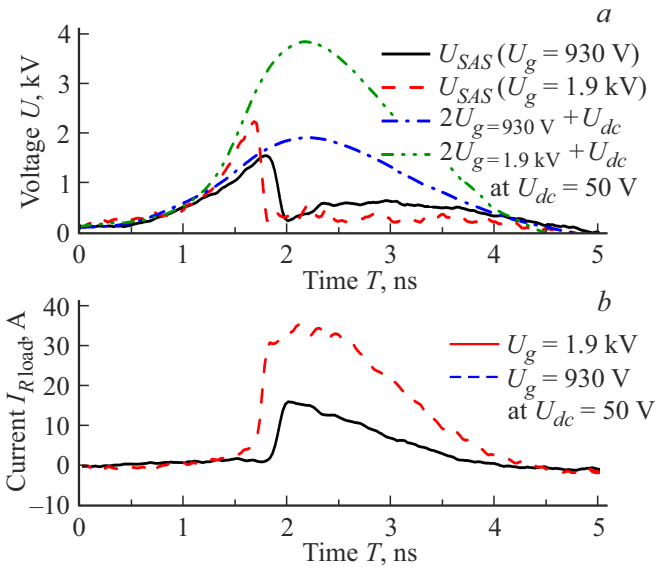

Figure 4. Oscillograms of (*a*) voltage pulses U_{SAS} on the structure and applied voltage pulses $2U_g + U_{dc}$ and (*b*) current I_{Rload} flowing through the structure at fixed DC bias $U_{dc} = 50$ V and two pulse amplitudes $U_g = 930$ V and 1.9 kV.

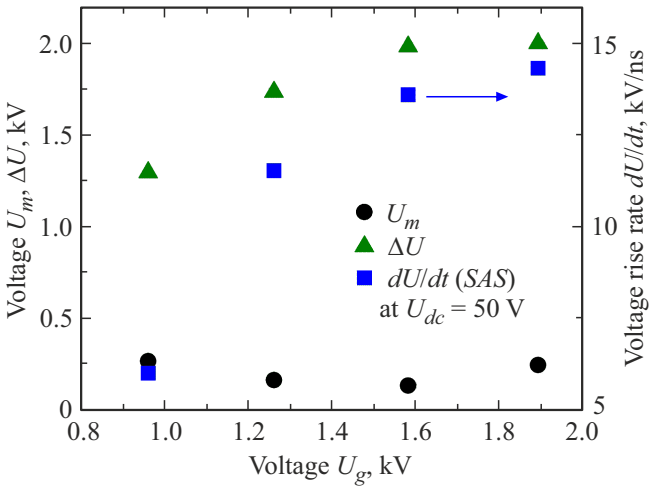

Figure 5. Dependences of switching rate dU/dt, voltage drop ΔU, and residual voltage U_m at different amplitudes of voltage pulse U_g applied to the sample and fixed bias voltage $U_{dc} = 50$ V.

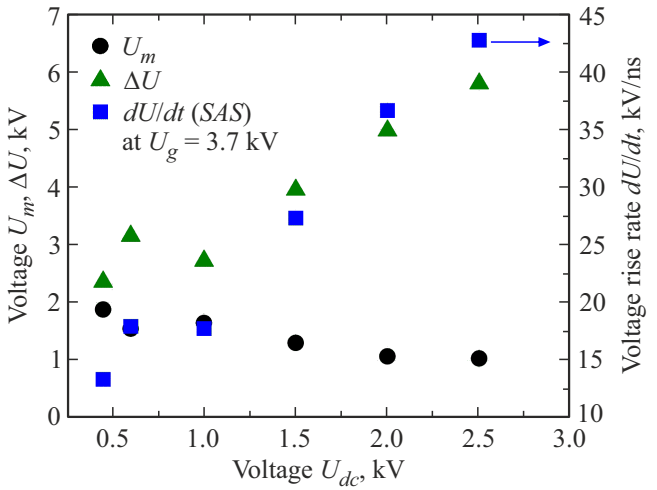

Figure 6. Dependences of switching rate dU/dt, voltage drop ΔU, and residual voltage U_m at different bias voltages U_{dc} and a fixed amplitude of voltage pulse $U_g = 3.7$ kV applied to the sample with base region thickness $W_B \approx 410\,\mu$m.

edge contour. The diameter of the sample at the p^+ and n^+ layer sides was 5 mm and 3 mm, respectively. Structures with similar parameters were discussed in [23] and used in generators with an output pulse amplitude of several tens of kilovolts. However, the authors of this study limited themselves to demonstrating the feasibility of switching such structures and their application in generators and did not examine them in detail.

Following the procedure established in experiments with the previous type of structures, we first investigated the dependences of switching parameters on the applied DC bias with voltage pulse U_g with an amplitude of 3.7 kV fed from the high-voltage generator. The obtained results are presented in Figure 6.

The obtained dependences of switching rate dU/dt, voltage drop ΔU across the structure, and residual voltage U_m at the structure demonstrate that all switching parameters improve as the DC bias increases. The growth of dU/dt and ΔU is near-linear within the studied range of DC bias voltages and does not reach saturation.

A switching rate $dU/dt = 42.7$ kV/ns was achieved, and the maximum voltage drop was $\Delta U = 5.8$ kV. The obtained results reveal the potential for a significant increase in power switched by a single diode structure.

The next series of experiments was carried out with DC reverse bias $U_{dc} = 2.5$ kV and varying amplitude $U_g = 2.7-3.7$ kV of the high-voltage generator pulse. With this bias voltage, the structure did not switch if the amplitude of applied voltage pulses was < 2.7 kV. The switching characteristics are shown in Figure 7.

It can be seen from Figure 7 that the values of residual voltage U_m and voltage drop ΔU across the structure vary insignificantly with an increase in the amplitude of the triggering high-voltage pulse, while switching rate dU/dt increases almost linearly at first and tends to saturation at levels > 3.2 kV.

It should also be noted that the sample was destroyed when the minimum amplitude of a pulse from the generator and the maximum DC bias $U_{dc} = 2.5$ kV were applied. The probable cause of destruction is filamentation of the current. All the oscillograms were recorded in a single triggering real time mode. The interval between switching events was no less than ten seconds; thus, heating of the sample and an increase in its average temperature were excluded. Destruction was observed after several switching cycles in this mode. No gradual degradation of parameters from pulse to pulse was noted throughout the entire experiment, i. e., right up to the last pulse that resulted in the destruction of the sample.

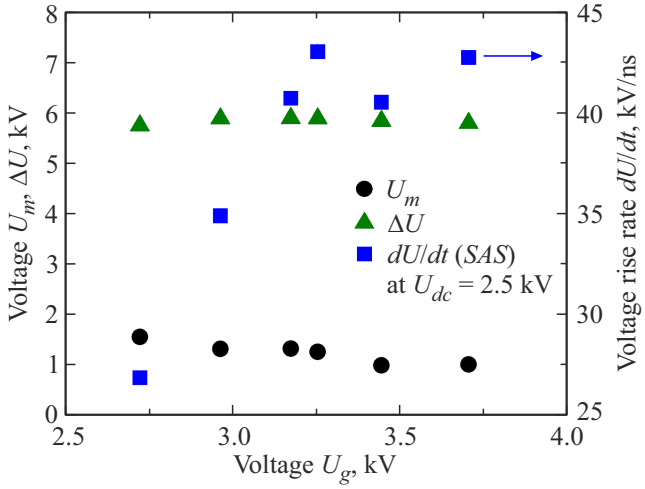

Figure 7. Dependences of switching rate dU/dt, voltage drop ΔU, and residual voltage U_m on the amplitude of the voltage pulse from the high-voltage generator at DC bias voltage $U_{dc} = 2.5$ kV for the structure with base region thickness $W_B \approx 410\,\mu$m.

4. Conclusion

A novel method for measuring fast processes in semiconductor high-voltage switches, which provides an opportunity to apply high DC and pulse voltages to the examined structures and record the pulse voltage across the structures and current flowing through them with high accuracy and high temporal resolution without using shunts and resistive dividers, was developed and tested. The proposed test bench made it possible to study samples at high DC and pulse voltages (up to several kilovolts) and high currents (up to several hundred amperes) with a temporal resolution better than 100 ps.

The characteristics of switching upon delayed impact ionization of silicon p^+-n-n^+ structures with base region thicknesses of $W_B \sim 100\,\mu$m and $\sim 410\,\mu$m were investigated with applied DC and pulse voltages varying within ranges wider than those examined in earlier studies. It was demonstrated that the data obtained in overlapping parameter ranges are in agreement with the results published earlier. However, new data obtained by examining the process of delayed impact ionization over a much wider range of parameters are unexpected in the context of current understanding of delayed impact ionization. Specifically, an increase in DC voltage to > 100 V had a negative effect on switching parameters dU/dt, ΔU, and U_m of the structures with an n-base width of $100\,\mu$m. At the same time, an increase in DC bias of structures with an n-base $410\,\mu$m in thickness led to an almost proportional increase in switching rate dU/dt and an almost twofold reduction in residual voltage U_m. These two types of diode structures also have fundamentally different dependences of switching parameters dU/dt and ΔU on the applied voltage pulse amplitude.

A switching rate $dU/dt \sim 42.7$ kV/ns was achieved at a DC bias voltage of 2.5 kV for structures with an n-base thickness of $410\,\mu$m.

Conflict of interest

The authors declare that they have no conflict of interest.

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