Electrical properties of InP/InGaAs *pnp* heterostructure–emitter bipolar transistor

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The dc performances of an InP/InGaAs *pnp* heterostructure-emitter bipolar transistor have been investigated by theoretical analysis and experimental results. Though the valence band discontinuity at InP/InGaAs heterojunction is relatively large, the addition of a heavy-doped as well as thin p^+-InGaAs emitter layer between *p*-InP confinement and n^+-InGaAs base layers effectively eliminates the potential spike at emitter–base junction, lowers the emitter–collector offset voltage, and increases the potential barrier for electrons, simultaneously. Experimentally, a high current gain of 88 and a low offset voltage of 54 mV have been achieved.

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1. Introduction

Over the past years, InP-based heterojunction bipolar transistors (HBTs) have been widely used in microwave performance applications such as optical communications, low $1/f$ noise characteristics, high-frequency circuit applications [1,2]. As compared with the GaAs-based HBTs, the major advantages of InP/InGaAs HBTs includes

1) lower surface recombination velocity,
2) lower turn-on voltage,
3) lower electron effective mass,
4) higher electron mobility, and
5) high etching selectivity between InP and InGaAs [3,4].

Previously, *npn* HBTs in combination with *pnp* HBTs had been employed for complementary integrated circuits and push-pull microwave amplifiers [5.6]. However, these applications were limited by low current gains of *pnp* HBTs resulting part from the low hole mobility. With respect to the conventional InP/InGaAs *pnp* HBTs, the large conduction band discontinuity ($\Delta E_c \approx 0.271$ eV) could introduce excellent confinement effect for electron. However, the potential spike at base-emitter (B-E) junction caused by the relatively large valence band discontinuity ($\Delta E_v \approx 0.345$ eV) will result in a relatively large emitter-collector offset voltage (ΔV_{EC}) and increase unnecessary power consumption in digital circuit applications [7].

Though the compositionally graded emitter has been made to smooth out the spike for the AlGaAs/GaAs *npn* HBTs [8], it is not applicable for the InP/InGaAs material systems owing to the lattice matched limitation. Another, the setback *npn* HBTs using an undoped setback layer at B-E junction can lower the energy band at the emitter side [9]. However, the potential spike might be not completely eliminated unless the setback layer is thick enough. Then it will increase the spacer recombination currents and degrade the current gain. Furthermore, an improved device structure, i. e., *npn* heterostructure-emitter bipolar transistor (HEBT), has been realized to eliminate the potential spike by way of the insertion of a small energy-gap emitter layer between confinement and base layers [10–12]. The confinement layer could keep good confinement effect for holes injecting from base into the emitter and the small energy-gap emitter layer helps to decrease the potential spike. Nevertheless, if the small energy-gap emitter layer is too thick, the transistor will act with inferior confinement effect. Then, the charge storage in neutral-emitter region enhances the base recombination current and increases the total base current [11].

Until now, only few InP/InGaAs *pnp* HBTs were reported and the offset voltage were relatively large [13,14]. In this article, the structure design and dc characteristic of an InP/InGaAs *pnp* HEBT are demonstrated for substantially decreasing the potential spike. Excellent device performances including a high current gain and a low offset voltage are depicted.

2. Experiments

The studied InP/InGaAs *pnp* HEBT was grown on an (100) oriented semi-insulating InP substrate by low-pressure metal-organic chemical vapor deposition (LP-MOCVD). The device's structure consisted of

a $0.5\,\mu$m $p^+ = 10^{19}$cm^{-3} $In_{0.53}Ga_{0.47}As$ subcolector layer,

a $0.5\,\mu$m $p^- = 5 \cdot 10^{16}$ cm^{-3} $In_{0.53}Ga_{0.47}As$ collector layer,

a 500 Å $n^+ = 5 \cdot 10^{18}$ cm^{-3} $In_{0.53}Ga_{0.47}As$ base layer,

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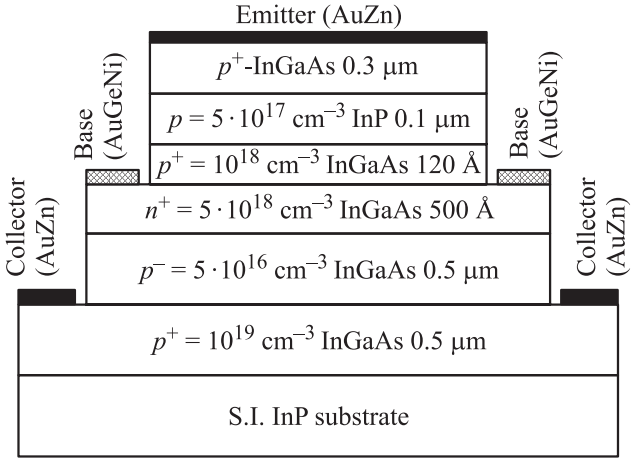

Figure 1. Schematic cross section of the experimental device.

a 120 Å $p^+ = 10^{18}$ cm^{-3} $In_{0.53}Ga_{0.47}As$ emitter layer,
a 0.1 μm $p = 5 \cdot 10^{17}$ cm^{-3} InP confinement layer, and
a 0.3 μm $p^+ = 10^{19}$ cm^{-3} $In_{0.53}Ga_{0.47}As$ cap layer.

Trimethylindium (TMI), trimethylgallium (TEG), phosphine (PH_3), and arsine (AsH_3) were used as In, Ga, P, and As source, respectively. Silane (SiH_4) and dimethylzinc (DMZ) were used as the dopants for n and p layers, respectively. After the epitaxial growth, the conventional photolithography, vacuum evaporation and wet selective etching processes were used to fabricate the device. The n- and p-type ohmic contact metals were AuGeNi and AuZn, respectively. The emitter area was $50 \times 50\,\mu m^2$. Schematic cross section of the studied InP/InGaAs pnp HEBT is shown in Fig. 1.

3. Results and discussion

By solving the Poisson's equation, the band diagrams near the emitter-base (E-B) junction at equilibrium and under forward biases for the experimental device are plotted in Fig. 2. Obviously, the potential spike at E-B junction can be completely eliminated due to the employments of a heavy-doped as well as thin p^+-InGaAs emitter layer between p-InP confinement and n^+-InGaAs base layers, even at $V_{EB} = 0.2$ V. The thin p^+-InGaAs emitter layer may help to promote the energy band at emitter side and increase the effective potential barrier for electrons. Thus, the transistor actions with high emitter injection efficiency and current gain are expectable. Usually, the offset voltage can be expressed as [7]

$$\Delta V_{EC} = \Delta V + \frac{KT}{q} \ln\left(\frac{1}{\alpha_t \gamma_C}\right), \qquad (1)$$

where ΔV, α_t and γ_C are the potential spike, the forward transport factor, and the collector injection efficiency, respectively. The offset voltage could be decreased with the elimination or reduction of the potential spike at E-B junction. The influence of the thin p^+-InGaAs emitter layer on the potential spike is discussed as follows.

Fig. 3 shows the varieties of valence-band diagrams near the depleted E-B junction for the 120 Å-emitter layers with the different doped concentrations at equilibrium. Cleanly, than the beavier doped concentration is, the higher the valence band energy at the emitter side is. As found in the figure, the doped concentration must be greater that $5 \cdot 10^{17}$ cm^{-3} and then the potential spike at E-B junction could be substantially removed. In additon, at equilibrium the varieties of valence-band diagrams near the depleted E-B junction for the device with different thickness of the p^+-InGaAs emitter layer, which the doping concentration of p^+-InGaAs emitter layer is fixed as 10^{18} cm^{-3}, are shown in

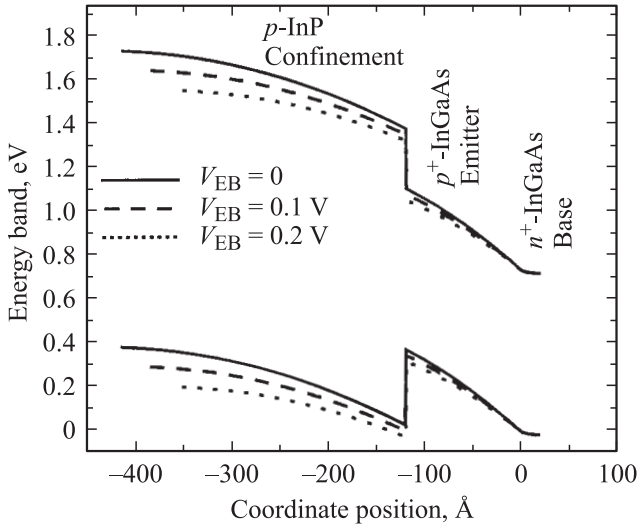

Figure 2. Band diagrams near the emitter-base junction of the experimental device at equilibrium and under forward biases V_{EB}.

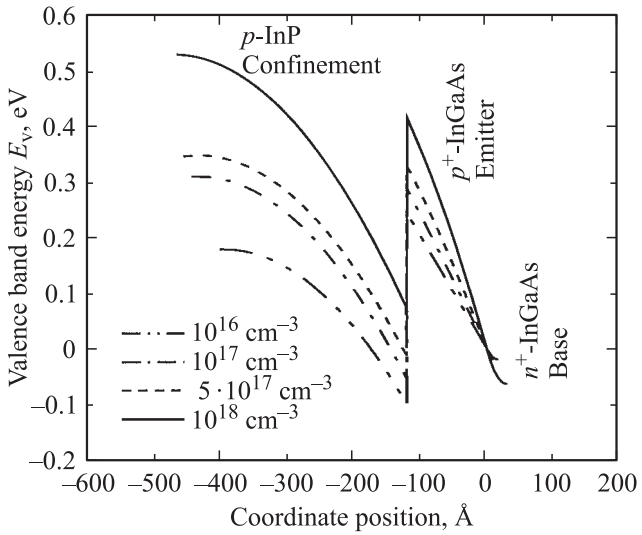

Figure 3. Valence-band diagrams near the depleted emitter-base junction for the p^+-InGaAs emitter layer with different doped concentrations at equilibrium. The thickness of emitter layer is 120 Å.

Fig. 4. Apparently, the potential spike could not be removed until the p^+-InGaAs emitter layer is increased up to 120 Å. A thicker p-InGaAs emitter layer can further promote the valence band at emitter side, but too thick InGaAs layer will result in a large space-charge recombination current and degrade the current gain. Therefore, 120 Å $p^+ = 10^{18}$ cm^{-3} $In_{0.53}Ga_{0.47}As$ emitter layer of the experimental device is proper to achieve high current gain and low offset voltage, simultaneously.

The typical common-emitter current–voltage (I–V) characteristics of the experiment device at room temperature, measured by an HP4155B semiconductor parameter analyzer, are illustrated in Fig. 5. The base current I_B is applied by $-5\,\mu$A/step. The transistor's performance exhibits a

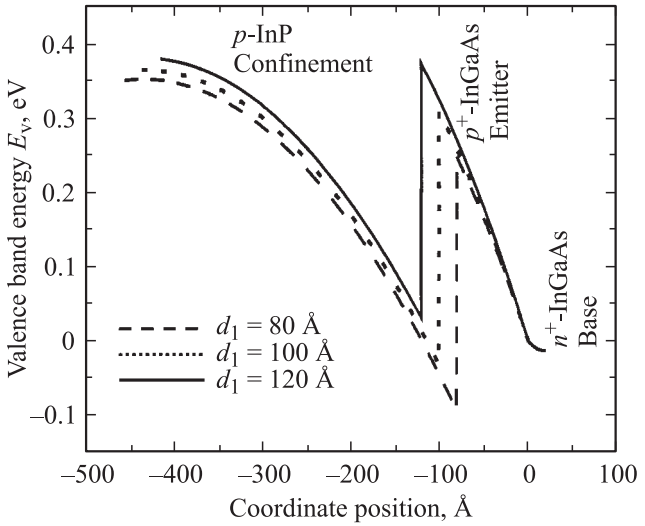

Figure 4. Varieties of valence-band diagrams near the depleted emitter-base junction of the devices with different thickness of the p^+-InGaAs emitter layer at equilibrium. The doping concentration of p^+-InGaAs emitter layer is 10^{18} cm^{-3}.

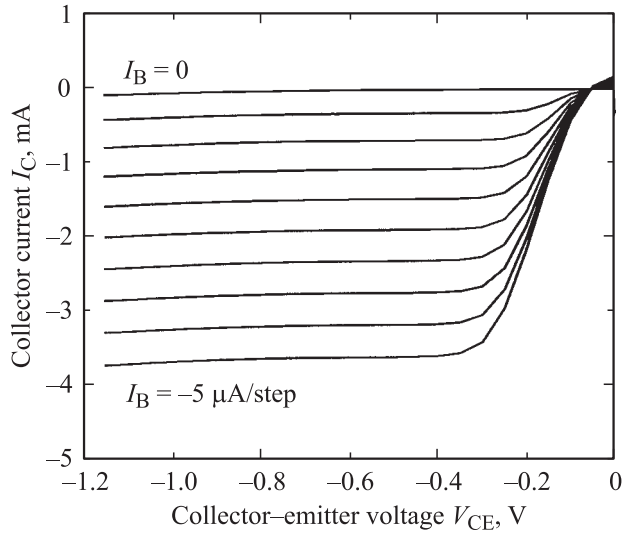

Figure 5. Common-emitter current–voltage characteristic of the experimental device.

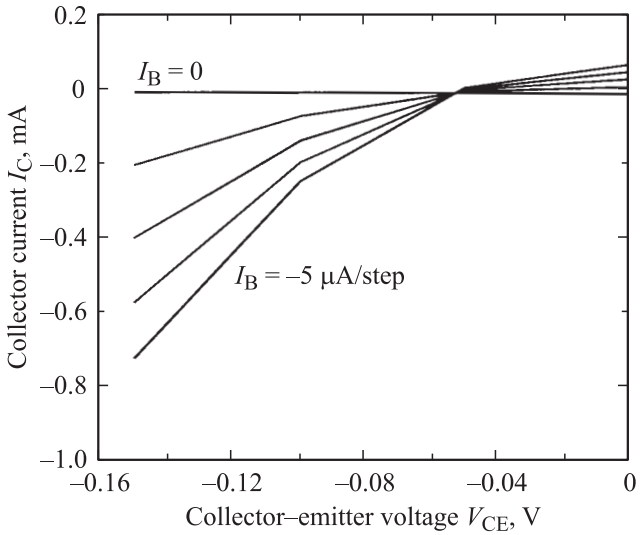

Figure 6. Enlarged view of the current–voltage characteristic near the origin.

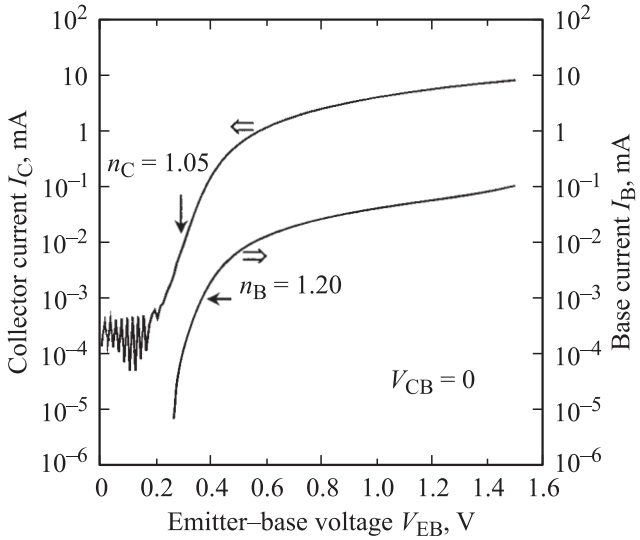

Figure 7. Measured Gummel plots of the experimental device.

maximum (in absolute value) collector current of -3.7 mA and a maximum current gain of 88, respectively. Fig. 6 depicts the enlarged view near the origin of the I–V characteristic. A relatively low offset voltage of only 54 mV is observed at $I_B = -5\,\mu$A. To our knowledge, the offset voltage of the studied device is the lowest value among of the reported InP/InGaAs *pnp* HBTs [13,14].

Fig. 7 illustrates the Gummel plots of the studied device at $V_{CB} = 0$. The ideality factor n_C for collector current is nearly equal to unity at low current level. This means that the thermionic-emission and diffusion mechanisms dominate the hole transportation across the E-B junction. Also, a low turn-on voltage of E-B junction about 0.37 V is obtained at the current level of 0.1 mA, attributed to the reduction of the potential spike and the use of the small energy-gap

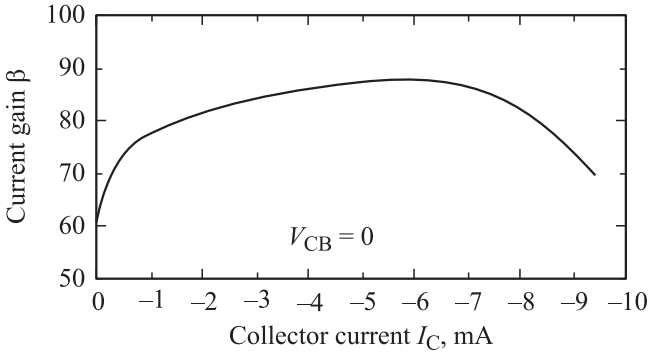

Figure 8. Current gain as a function of collector current at $V_{CB} = 0$.

InGaAs base. This low junction turn-on voltage can reduce the operating voltage and decrease the power consumption in circuit applications. On the other hand, the ideality factor n_B for base current is equal to 1.2 at low current level, which means that the addition of a thin p^+-InGaAs emitter layer does not increase the base recombination current excessively and degrade the device performance. The dependence of current gain on the collector current at $V_{CB} = 0$ is shown in Fig. 8. Based on the reduction of potential spike at the E-B junction, a high current gain is observed at low current level. Thus, the studied device exhibiting high device linearity, i. e., current gain β versus collector current I_C, is proper for linear amplifier applications.

4. Conclusion

The characteristics of the InP/InGaAs *pnp* HEBT have been fabricated and investigated. The structure design of the thin emitter layer is also illustrated. A high current gain of 88 and a low offset voltage of 54 mV are achieved by the use of a heavy-doped as well as thin p^+-InGaAs emitter layer at E-B junction. Consequently, the demonstrated device shows good potentiality for linear amplifiers and low power complementary integrated circuit applications.

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