High-performance InGaP/GaAs *pnp* δ-doped heterojunction bipolar transistor

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In this article, a novel InGaP/GaAs *pnp* δ-doped heterojunction bipolar transistor is first demonstrated. Though the valence band discontinuity at InGaP/GaAs heterojunction is relatively large, the addition of a δ-doped sheet between two spacer layers at the emitter–base (E–B) junction effectively eliminates the potential spike and increases the confined barrier for electrons, simultaneously. Experimentally, a high current gain of 25 and a relatively low E–B offset voltage of 60 mV are achieved. The offset voltage is much smaller than the conventional InGaP/GaAs *pnp* HBT. The proposed device could be used for linear amplifiers and low-power complementary integrated circuit applications.

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1. Introduction

Npn heterojunction bipolar transistors (HBTs) in combination with *pnp* HBTs have been used for the implementations of low-power complementary integrated circuits and push-pull microwave amplifiers [1,2]. Over the past years, *npn* InGaP/GaAs HBTs have received considerable interest in the replacement of AlGaAs/GaAs material systems due to

1) the large valence band discontinuity ($\Delta E_v \approx 0.35$ eV) to conduction band discontinuity ($\Delta E_c \approx 0.15$ eV) ratio of InGaP/GaAs material system.

2) high etching selectivity between InGaP and GaAs layers,

3) low density of DX center, and

4) low surface recombination velocity of InGaP layer [3,4].

However, the performances of complementary HBT-based circuits are severely limited by the *pnp* transistors due to the small current gain resulting part from the low hole mobility. Previously, the first InGaP/GaAs *pnp* HBT had been demonstrated [5]. Because of the large ΔE_v value at emitter–base (E–B) heterojunction giving rise to a potential spike blocking the hole injection from the emitter across the base, the device exhibited a notable emitter–collector (E–C) offset voltage (ΔV_{EC}) of about 800 mV. It might increase the undesirable power consumption in digital circuit applications [5,6].

In order to decrease the offset voltage, some improved *npn* transistors, e.g., setback HBTs [7], heterostructure-emitter bipolar transistor (HEBTs) [8], and δ-doped heterojunction bipolar transistor (δ-HBTs) [9,10], have been well demonstrated. As to the setback *npn* HBTs, an undoped setback layer added at base–emitter (B–E) junction is entirely depleted and halps to lower the energy band at the emitter side. However, the potential spike might be not completely eliminated unless the setback layer is thick enough. Then, it will increase the spacer recombination currents and degrade the current gain. For the *npn* HEBTs, a thick as well as small energy-gap *n*-type emitter layer is added at B–E junction for reducing the offset voltage. Nevertheless, if the small energy-gap emitter layer is too thick, the transistor will perform with inferior confinement effect. Then, the charge storage in neutral-emitter region also enhances the base recombination current and increases the total bese current. In other words, though a low offset voltage is achieved, the current gain might be degraded particularly under large forward B–E voltage [8]. On the other hand, if a thinner as well as small energy-gap emitter layer is employed, the device will seve as conventional HBTs and the undesirable offset voltage is considerably large. Previously, AlGaAs/GaAs and InGaP/GaAs *npn* δ-HBTs have been proposed and demonstrated. Due to the elimination of potential spike by the insertion of a δ-doped sheet at B–E junction, a low offset voltage and a high current gain were achieved, simultaneously [9,10].

In this article, we report a new InGaP/GaAs *pnp* HBT with a heavily δ-doped sheet between two spacer layers at hte E–B junction for more effectively reducing the potential spike and increasing the confined barrier for electrons. Excellent DC performances including a high current gain, a low offset voltage, and good device linearity are demonstrated.

2. Experiments

The device structure was grown on an (100) oriented semi-insulating GaAs substrate by a low-pressure metal-organic chemical vapor deposition (MOCVD) system. The

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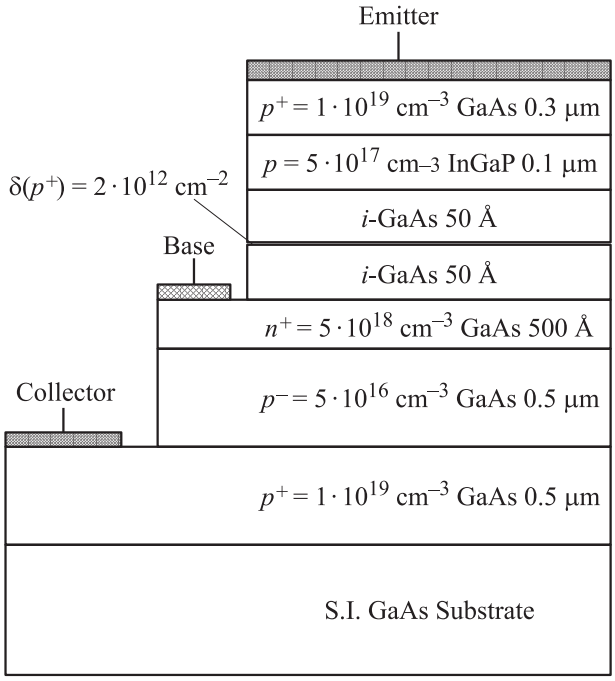

Fig. 1. Cross section of the studied InGaP/GaAs *pnp* δ-doped HBT.

eptaxial layers included a $0.5\,\mu$m $p^+ = 10^{19}\,\text{cm}^{-3}$ GaAs subcollector layer, a $0.5\,\mu$m $p^- = 5 \cdot 10^{16}\,\text{cm}^{-3}$ GaAs collector layer, a 500 Å $n^+ = 5 \cdot 10^{18}\,\text{cm}^{-3}$ GaAs base layer, a 50 Å *i*-GaAs spacer layer, a $p^+ = 2 \cdot 10^{12}\,\text{cm}^{-2}$ δ-doped sheet, a 50 Å *i*-GaAs space layer, a $0.1\,\mu$m $p = 5 \cdot 10^{17}\,\text{cm}^{-3}$ InGaP emitter layer, and a $0.3\,\mu$m $p^+ = 10^{19}\,\text{cm}^{-3}$ GaAs cap layer. Trimethylindium (TMI), trimethylgallium (TMG), phosphine (PH_3), and arsine (AsH_3) were used as the In, Ga, P, and As sources, respectively. The dopants used for *n* and *p* layers were silane (SiH_4) and dimethylzine (DMZ), respectively. After the epitaxial growth, the conventional photolithography, vacuum evaporation and wet selective etching processes were used to fabricate the device. The *n*- and *p*-type ohnic contact metals were AuGeNi and AuZn, respectively. Fig. 1 shows the cross section of the studied device. The emitter area was $50 \times 50\,\mu\text{m}^2$.

3. Experimental results and discussion

Under the transistor operation, electrons in the base are substantially confined by the ΔE_c at *p*-InGaP/*i*-GaAs heterojunction. Furthermore, the additions of a δ-doped sheet and two spacer layers at the E–B junction also helps to enhance the confinement effect for electrons. This will suppress electron back injection form the base into the emitter. On the other hand, though the ΔE_v value (0.35 eV) at the InGaP/GaAs heterojunction is considerably large, the $\delta(p^+)$-doped sheet and two spacer layers could promote the energy band at emitter side and reduce the potential spike blocking the holes injection efficiency could be substantially increased. The offset voltage can be ixpressed as [11]

$$\Delta V_{EC} = \Delta V + \frac{kT}{q} \ln\left(\frac{1}{\alpha_T/\gamma_C}\right), \qquad (1)$$

where ΔV, α_T, and γ_C are the potential spike, the forward transport factor, and the collector injection efficiency, respectively. The offset voltage could be decreases with the elimination or reduction of the potential spike at E–B junction. At equilibrium, a comparison of valence band diagrams near the E–B junction for the InGaP/GaAs *pnp* HBTs with different δ-doped levels is illustrated in Fig. 2. The heavier the δ-doped density is, the higher the valence band energy at the emitter side is. It can be seen that the potential spike can be eliminated completely, when the δ-doped level is incresed up to $2 \cdot 10^{12}\,\text{cm}^{-2}$.

The typical common-emitter current–voltage (I–V) characteristic at room temperature, measured by an HP4155B semiconductor parameter analyzer, is shown in Fig. 3, *a*. The base current I_B is applied by $-20\,\mu$A/step. The device performances exhibit a maximum collector current of -1.75 mA and a maximum current gain of 25, respectively. Though the base to emitter doping ratio of the studied device is larger than the former InGaP/GaAs *pnp* HBT, the current gains of the two devices are close to the same [5]. Fig. 3, *b* depicts the enlarged view naer the origin of the *I*–*V* characteristic. A relatively low offset voltage of only 60 mV at $I_B = -20\,\mu$A is observed. The value is much smaller than that of the InGaP/GaAs *pnp* HBT without the δ-doped design [5].

Fig. 4 illustrates the Gummel plots of the studied device at $V_{CB} = 0$ V. The ideality factor n_C for collector current is

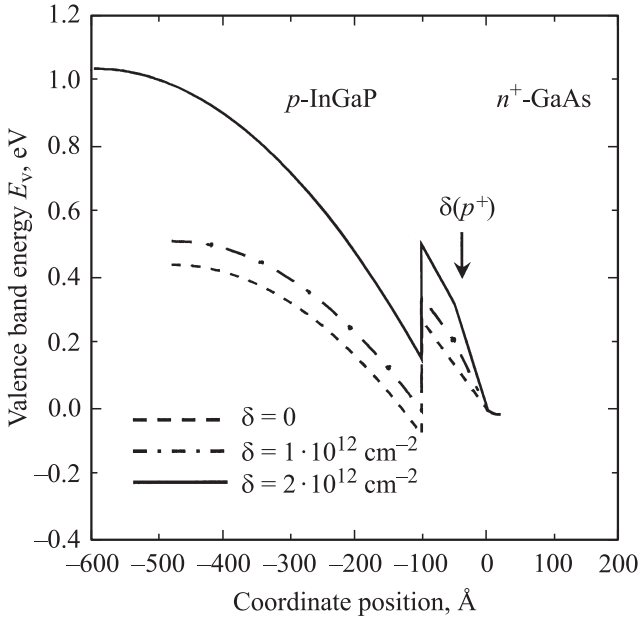

Fig. 2. Valence band diagrams near the emitter–base junction of the devices with different δ-doped levels at equilibrium.

nearly equal to unity at low current levels. This means that the thermionic-emission and diffusion mechanisms dominate the hole transportation across the E–B junction. Also, a low E–B turn-on voltage of about 1.08 V is obtained at the current level of 0.1 mA due to the reduction of the potential spide. The low turn-on value could reduce the operation voltage and decrease the power consumption in digital circuit applications. On the other hand, the ideality factor for base current n_b is equal to 1.2 at low current levels, which means that the additions of a δ-doped sheet and two spacer layers do not increase the base recombination current excessively and degrade the device performance. Based on the elimination of the potential spike at the E–B junction, a high current gain at low current level is observed. Thus, the studied device exhibiting high device linearity, i. e., current gain β versus collector current I_C, is proper for linear amplifier applications.

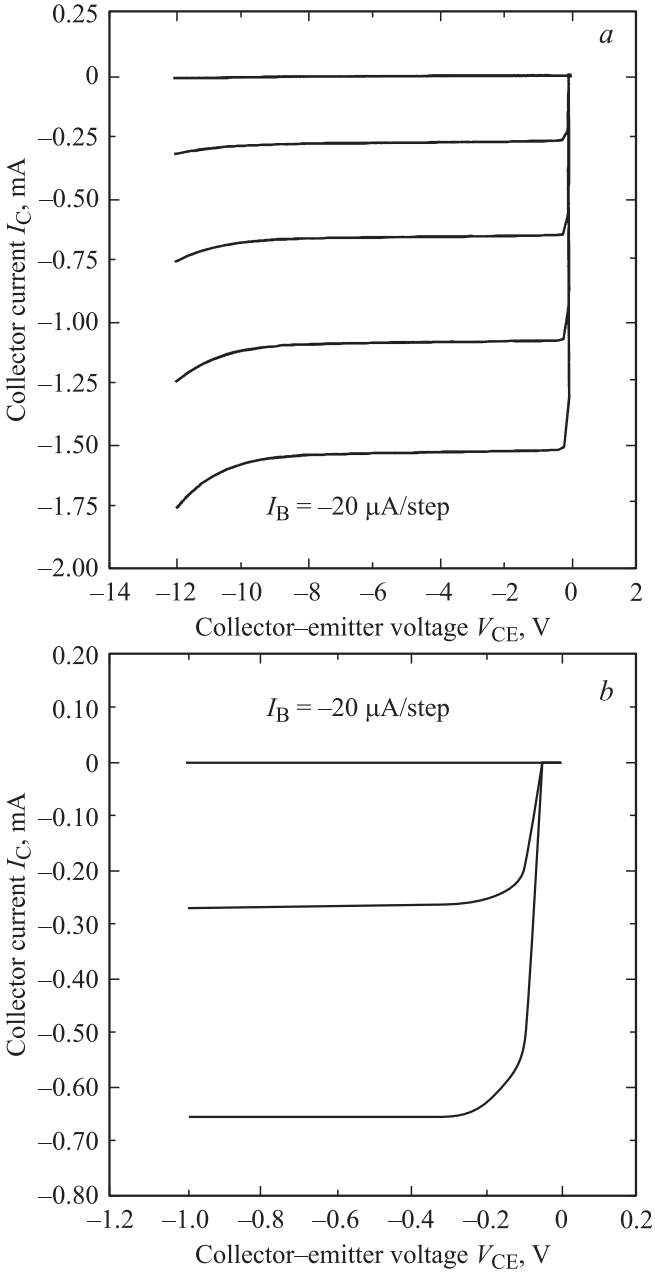

Fig. 3. *a* — common-emitter current–voltage characteristic of the experimental device; *b* — enlarged view of the current–voltage characteristic near the origin.

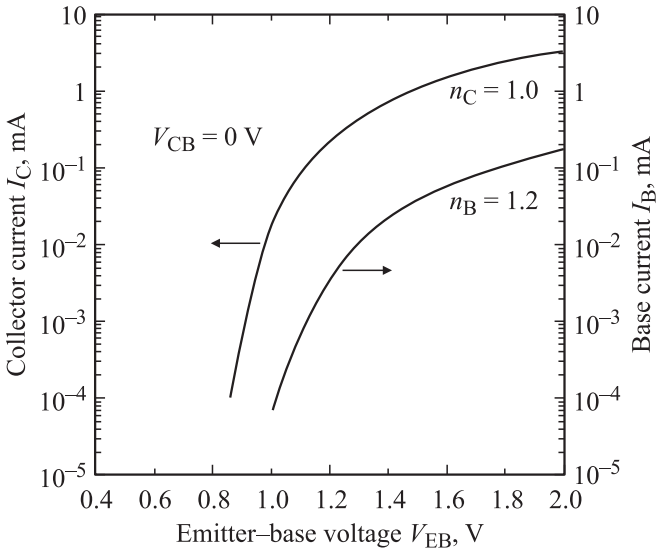

Fig. 4. Gummel plots of the experimental device.

4. Conclusion

In summary, we have successfully fabricated and demonstrated a high-performamce InGaP/GaAs pnp δ-doped HBT. Although the ΔE_v value at InGaP/GaAs heterojunction is relatively large, a high current gain ($\beta = 25$) and a low offset voltage (60 mV) are achieved by the employments of a δ-doped sheet and two spacer layers at E–B junction. Consequently, the good performances provide a great promise for linear amplifier and low-power complementary integrated circuit applications.

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