InGaP/InGaAs Doped-Channel Direct-Coupled Field-Effect Transistors Logic with Low Supply Voltage

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InGaP/InGaAs doped-channel direct-coupled field-effect transistor logic (DCFL) with relatively low supple voltage is demonstrated by two-dimensional analysis. In the integrated enhancement/depletion-mode transistors, subband and two-dimensional electron gas (2DEG) are formed in the InGaAs strain channels, which substantially increase the channel concentration and decrease the drain-to-source saturation voltage. The integrated devices show high turn-on voltage, high transconductance, broad gate voltage swing, and excellent high frequency performance, simultaneously. Furthermore, the integrated devices exhibit large noise margins for DCFL application with low supply voltage of 1.5 V attributed from the relatively small saturation voltages of the studied integrated devices.

1. Introduction

Over the past years heterostructure field-effect transistors (HFETs), such as metal-semiconductor field-effect transistors (MESFETs) [1,2], doped-channel field-effect transistors (DCFETs) [3,4], and high electron mobility transistors (HEMTs) [5–7], etc., have been widely studied for microwave and digital circuit applications. It is especially essential for large signal circuit and linear amplifier applications in requiring high output current and broad gate operation range. As to the MESFETs, the high field around the metal-semiconductor interface causes the poor Schottky behaviors and it is difficult to achieve high gate turn-on voltage [1]. With respect to the HEMTs, these devices might show a sharp peak in transconductance as a function of gate voltage due to the onset of parallel conductance in high-bandgap doping materials, even though the output transconductance value could be relatively large [5]. Recently, the DCFETs have exhibited high current density, current linearity, and broad gate voltage swing [3,4]. The basic structure of DCFETs consists of a narrow bandgap doped channel and a wide bandgap undoped or low-doping barrier layer as an „insulator“ which could improve the gate Schottky characteristic and increase the breakdown voltage.

On the other hand, future high-speed computers and signal-processing systems require large-scale integrated (LSI) circuits that are very fast and have low power consumption. HEMTs had been demonstrated their high-speed performances for LSI-level complexity [6]. The supply voltage is required to be reduced for low power consumption. GaAs direct-coupled field-effect transistor logic (DCFL) circuits are one of the most suitable circuits for this purpose because of their high-speed performance and low-power consumption at low supply voltage [8,9]. However, the threshold voltage must be severely controlled in low supply voltage operation especially, otherwise the noise margins of the logic inverters will be drastically decreased.

In this paper, based on InGaP/InGaAs doped-channel field-effect transistors (DCFETs), the co-integrated enhancement/depletion-mode devices are addressed. The devices exhibit high gate turn-on voltage, high transconductance, lower saturation voltage, broad gate voltage swing, and excellent high frequency performance. Furthermore the relatively large noise margins in DCFL application with relatively low supply voltage are achieved.

2. Device structures

The structure of the integrated devices consisted of a $0.5\,\mu$m undoped GaAs buffer layer, a 100 Å ($n^+ = 2 \cdot 10^{18}\,\mathrm{cm}^{-3}$) $In_{0.2}Ga_{0.8}As$ lower doped-channel layer, a 150 Å undoped $In_{0.5}Ga_{0.5}P$ layer, a 100 Å ($n^+ = 2 \cdot 10^{18}\,\mathrm{cm}^{-3}$) $In_{0.2}Ga_{0.8}As$ upper doped-channel layer, a 200 Å undoped $In_{0.5}Ga_{0.5}P$ layer, and a 300 Å ($n^+ = 4 \cdot 10^{19}\,\mathrm{cm}^{-3}$) GaAs cap layer. The enhancement-mode region was formed after remove the uppermost two layers till the $In_{0.2}Ga_{0.8}As$ lower doped-channel layer appeared. For the depletion and enhancement devices, drain and source ohmic contacts were formed on the n^+-GaAs cap layer and the n^+-$In_{0.2}Ga_{0.8}As$ upper doped-channel layer, respectively. The Schottky gates were simultaneously formed on the 200 Å and 150 Å undoped $In_{0.5}Ga_{0.5}P$ layers for the depletion and enhancement-mode devices, respectively. A two-dimensional (2D) semiconductor simulation package, Atalas, was employed to analyze the energy band, DC and high-frequency performances [10]. The analysis takes into account the Poisson equation, continuity equation of electrons and holes, Shockley–Read–Hall (SRH) recombination, Auger recombination, and Boltzmann statistics, si-

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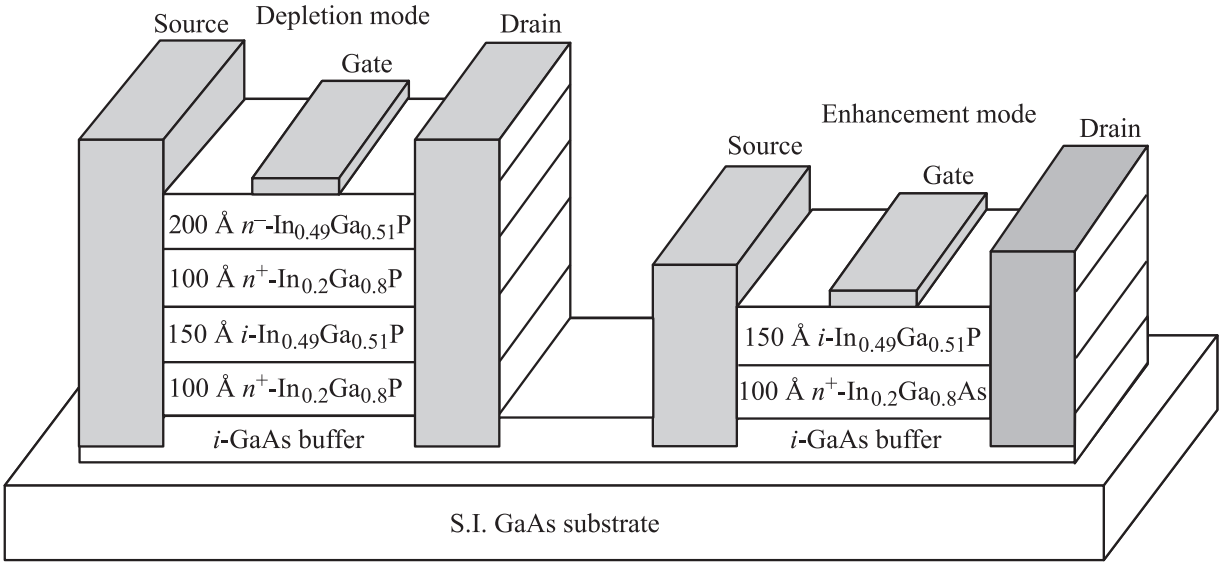

Fig. 1. Schematic cross section of the InGaP/InGaAs integrated doped-channel field-effect transistors.

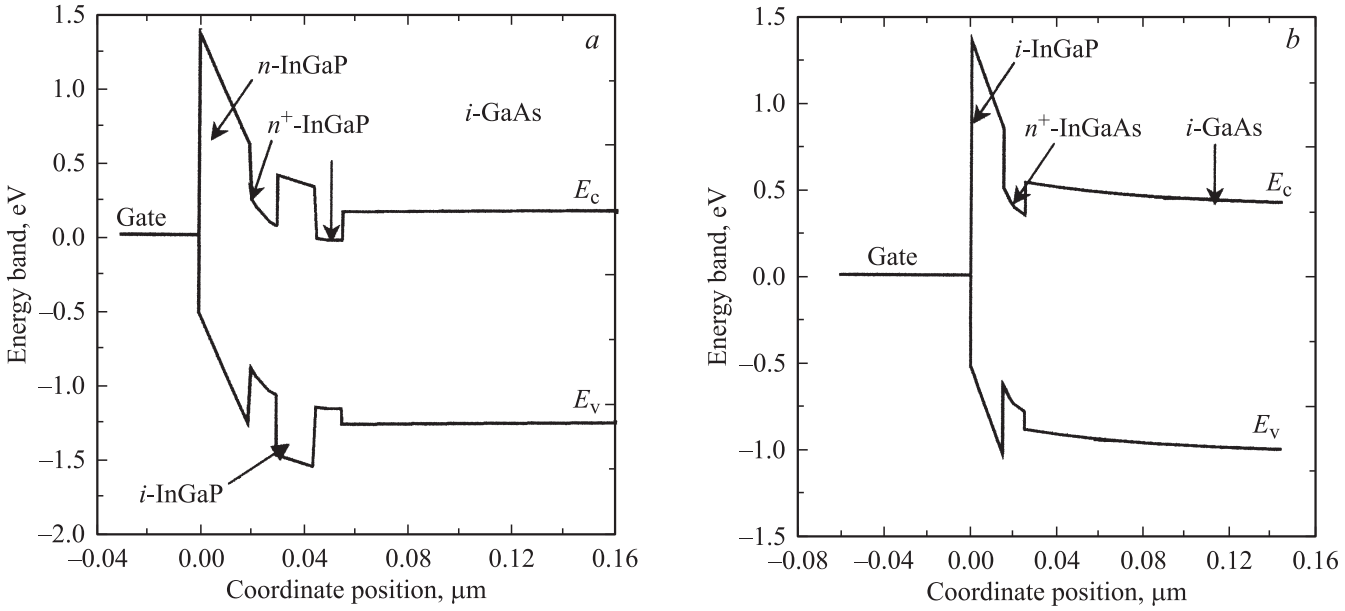

Fig. 2. Corresponding band diagrams at equilibriun of the depletion-mode device (a) and enhancement-mode device (b).

multaneously. The schematic cross section of the integrated devices is shown in Fig. 1. The gated dimension and the drain-to-source (D-S) spacing were $1 \cdot 70\,\mu m^2$ and $3\,\mu m$, respectively.

3. Results and discussion

3.1. Device characteristics

The corresponding band diagrams at equilibrium of the depletion and enhancement-mode devices are illustrated in Figs. 2, a and 2, b, respectively. As to the depletion-mode device, the upper doped-channel layer is entirely depleted and the depletion region is justly immersed into the lower doped-channel layer at equilibrium. Because the employment of the undoped $In_{0.5}Ga_{0.5}P$ gate layer and the considerable conduction band discontinuity ($\Delta E_c \approx 0.38$ eV) at $In_{0.5}Ga_{0.5}P/In_{0.2}Ga_{0.8}As$ heterojunction [3], it provides a large potential berrier preventing the injection of electrons from channel into gate electrode and increases forward gate operation voltage. Unlike the conventional MESFETs, subband and 2DEG in the lower InGaAs strain channel are formed, which could increase the channel concentration with the forward gate bias [11]. On the other hand, for

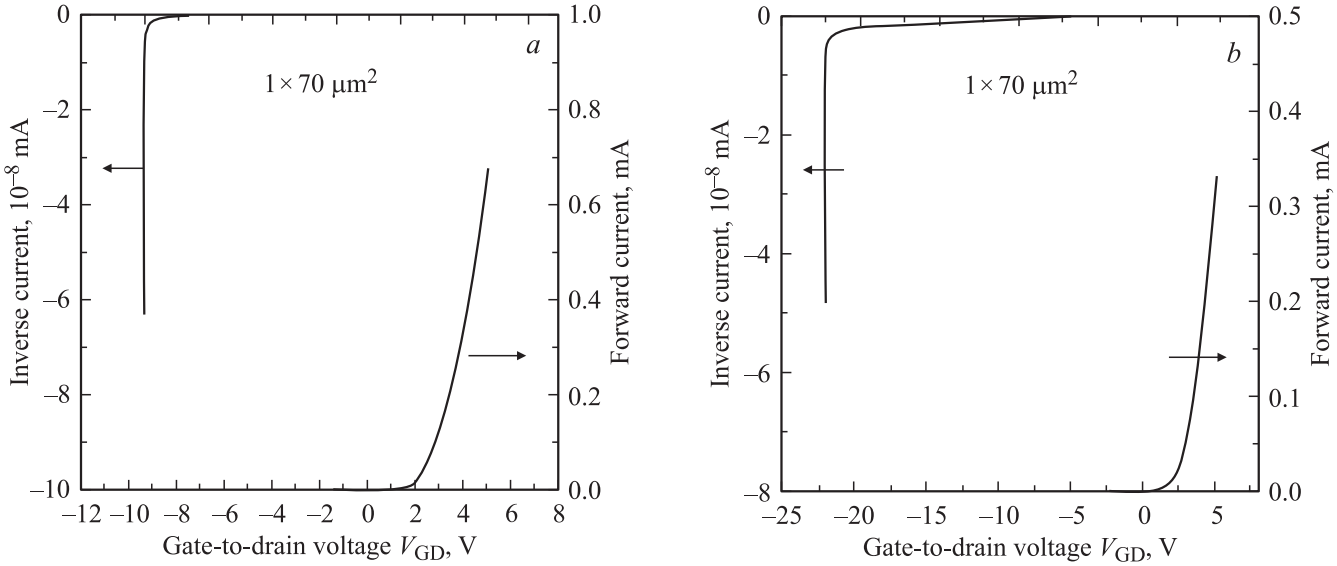

Fig. 3. Gate-to-drain current-voltage characteristics of the depletion-mode device (*a*) and enhancement-mode device (*b*).

the enhancement-mode device the doped-channel layer is completely depleted at equilibrium and the active channel appears under large forward bias. Similarly, subband and 2DEG are also formed in the lower InGaAs strain channel. Because the heavily doped-channel layers are relatively thin, the variety of gate depletion region with the gate bias is very small. Thus, relatively voltage-independent transconductances could be exhibited in the both devices.

The gate-to-drain (G-D) current-voltage (I-V) characteristics of the depletion and enhancement-mode devices are shown in Figs. 3, *a* and 3, *b*, respectively. The gate turn-on voltages are of 1.71 V (1.87 V) at gate current level of 0.01 mA for the depletion-mode (enhancement-mode) device. The large turn-on voltage can be attributed to the large gate potential barrier, and it could increase the gate voltage swing with the increase of the forward gate voltage for the integrated devices. In addition, the G-D breakdown voltages of about 9.42 V (22.1 V) at gate current level of 10 pA are observed for depletion-mode (enhancement-mode) device. This high breakdown voltage is mainly due to the use of the large energy-gap InGaP gate layer. Because the effective channel concentration of depletion-mode device with double channel layers is higher than that of the enhancement-mode device with single channel layer,

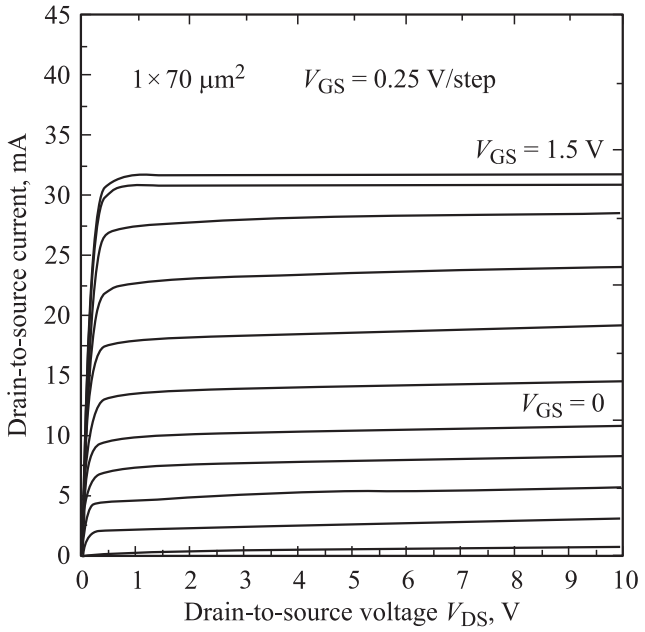

Fig. 4. Drain-to-source current-voltage characteristic of the depletion-mode device.

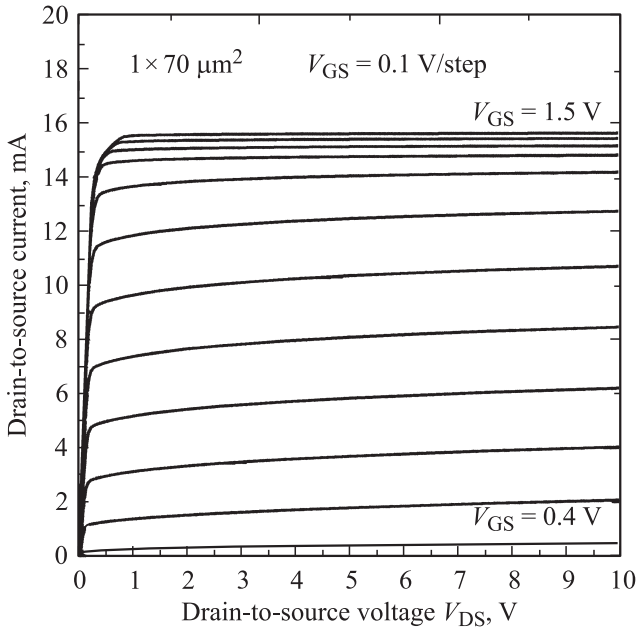

Fig. 5. Drain-to-source current-voltage characteristic of the enhancement-mode device.

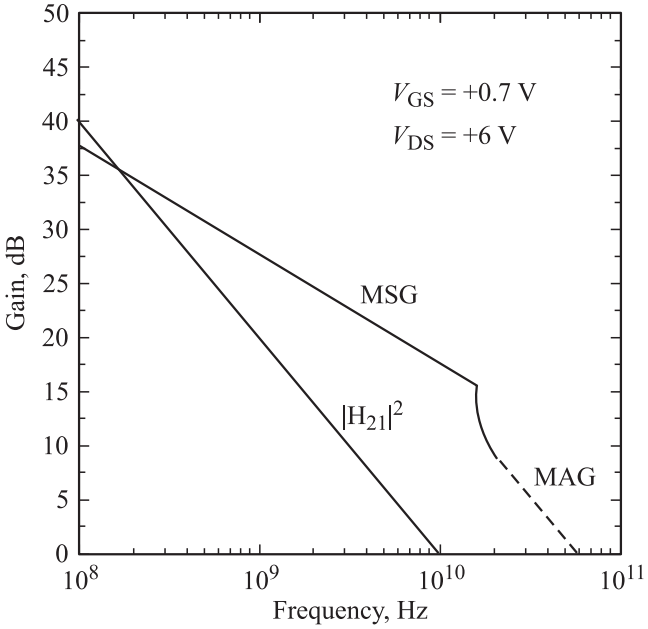

Fig. 6. Microwave performance of the depletion-mode device.

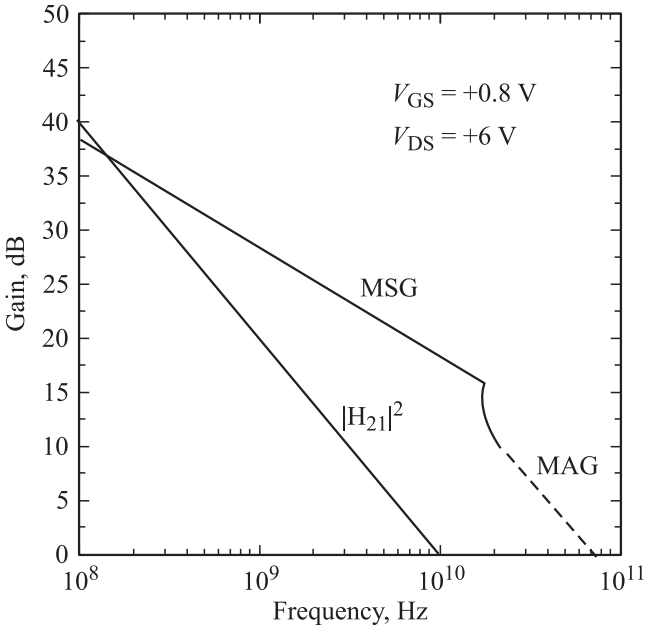

Fig. 7. Microwave performance of the enhancement-mode device.

the depletion-mode device shows the lower turn-on and breakdown voltages.

The drain-to-sourse I-V characteristics of the depletion and enhancement-mode devices are illustrated in Figs. 4 and 5, respectively. Most of carriers in the InGaAs strain channel may increase and be modulated under forward gate bias. In the depletion-mode device, the D-S saturation voltage of only 0.2 V at $V_{GS} = 0$ is observed. The saturation voltage is less than the previously reported DCFETs [3,4]. A large gate voltage swing from $V_{GS} = -1.25$ to $+1.5$ V is obtained. The large swing may reduce the third-harmonic distortion and perform as linear and large signal amplifier. Similar to the depletion-mode device, the enhancement-mode device also exhibit a large gate voltage swing from $V_{GS} = +0.3$ to $+1.5$ V. In addition, the drain saturation current density on 454 (223) mA/mm and the maximum transconductance values of 282 (327) mS/mm at $V_{DS} = +6$ V are obtained for depletion (enhancement) mode device. Under short channel approximation [12], the transconductance g_m can be expressed as

$$g_m \propto \frac{1}{d}. \quad (1)$$

Here d is the distance from gate to the resultant position of channel. Besause the d value of the enhancement-mode device is small, the transconductance is higher than the depletion-mode device.

Figures 6 and 7 depict the simulated microwave performance of the depletion and enhancement-mode devices, respectively. The maximum unity current gain cutoff frequency f_t of 10 (10.1) GHz and maximum oscillation frequency f_{max} of 60 (72) GHz are obtained for the depletion (enhancement) device. Because the transconductance of enhancement-mode device is higher than the depletion-mode device, it shows the better high-frequency characteristics.

3.2. DCFL application

For the DCFL application by using enhancement-mode device as driver and the depletion-mode device as the active load, the voltage transfer characteristic applied at supply voltages of 1.5 V is revealed in Fig. 8. The corresponding

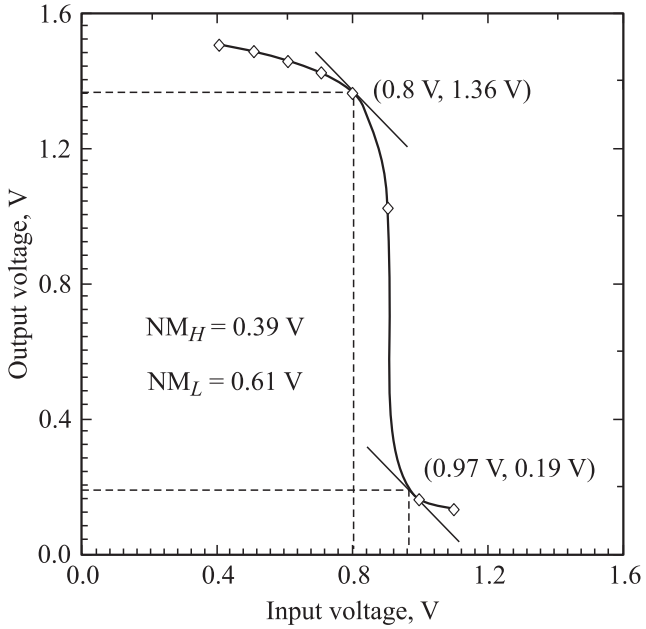

Fig. 8. Voltage transfer characteristic of the DCFL at supply voltages of 1.5 V.

voltage parameters, i. e., V_{IH}, V_{IL}, V_{OH}, V_{OL}, NM_H and NM_L, are 0.97, 0.8, 1.36, 0.19, 0.39, and 0.61, respectively. The above voltage values are defined as $dV_{out}/dV_{in} = -1$. The low power supply voltage is attributed from the low D-S saturation voltage. The low saturation voltage of the driver transistor effectively reduces the V_{OL} and V_{IH} values, while the low saturation voltage of the load transistor could increase the V_{OH} and V_{IL} values. Therefore, the noise margins of the inverter could be substantially increased. Consequently, the integrated DCFETs exhibit large noise margins for DCFL application resulted from the relatively small saturation voltages of the integrated devices.

4. Conclusion

In summary, the DC and high-frequency characteristics of the InGaP/InGaAs integrated DCFETs have been investigated. The integrated devices show relatively low D-S saturation voltage, high output current, and broad gate voltage swing, simultaneously. Furthermore, the large noise margins are achieved in the DCFL application. Consequently, the integrated devices provide a promise for linear amplification and direct-coupled FET logic applications.

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