Electrical characteristics of Au/*n*-GaAs structures with thin and thick SiO_2 dielectric layer

© H. Altuntas¶, S. Corekci+, S. Ozcelik*, S. Altindal*, M.K. Ozturk*

Department of Physics, Faculty of Sciences, Çankiri Karatekin University,
18100 Çankiri, Turkey
* Department of Physics, Faculty of Arts and Sciences, Gazi University,
06500 Ankara, Turkey
+ Department of Physics, Faculty of Arts and Sciences, Kirklareli University,
39000 Ankara, Turkey

(Получена 1 февраля 2011 г. Принята к печати 27 марта 2011 г.)

The aim of this study, to explain effects of the SiO_2 insulator layer thickness on the electrical properties of Au/*n*-GaAs Shottky barrier diodes (SBDs). Thin (60 Å) and thick (250 Å) SiO_2 insulator layers were deposited on *n*-type GaAs substrates using the plasma enhanced chemical vapour deposition technique. The current-voltage ($I-V$) and capacitance-voltage ($C-V$) characteristics have been carried out at room temperature. The main electrical parameters, such as ideality factor (n), zero-bias barrier height (ϕ_{Bo}), series resistance (R_s), leakage current, and interface states (N_{ss}) for Au/SiO_2/*n*-GaAs SBDs have been investigated. Surface morphologies of the SiO_2 dielectric layer was analyzed using atomic force microscopy. The results show that SiO_2 insulator layer thickness very affects the main electrical parameters. Au/*n*-GaAs SBDs with thick SiO_2 insulator layer have low leakage current level, small ideality factor, and low interface states. Thus, Au/*n*-GaAs SBDs with thick SiO_2 insulator layer shows better diode characteristics than other.

1. Introduction

Metal-oxide-semiconductor type Schottky barrier diodes (SBDs) are of great importance since they are used for the semiconductor devices. Existance of an insulator or oxide layer between metal and semiconductor can have strong influence the device properties as well as interface state density (N_{ss}), Schottky barrier heights (SBHs), ideality factor (n), and leakage current level [1–10]. GaAs is one of the $A^{III}B^{V}$ semiconductor compounds and its electrical properties which are superior to those of silicon. Due to GaAs has a higher saturated electron velocity and higher electron mobility, allowing devices made from it for high frequency and low power applications [11–14]. Since these benefits, much attention has been focused on the fabrication of GaAs based oxide devices with various insulator layers such as plasma enhanced chemical vapor deposition (PECVD) SiO_2. Some studies [15–19] inspected the effects of the presence of an interfacial oxide layer and the interface states on the behavior of SBDs, and extracted the density distribution of interface states in the semiconductor band gap from the forward-bias current–voltage ($I-V$) characteristics. Also, in our previous works [20,21], we showed the effects of the interfacial insulator layer on the properties of these devices with thin SiO_2 dielectric film.

In this study, thin and thick SiO_2 dielectric layers deposited on high quality *n*-type GaAs semiconductor substrate to explain effects of dielectric layer thickness on electrical parameters fo Au/SiO_2/*n*-GaAs SBDs. We calculated main electrical parameters such as $n\phi_{Bo}$ and R_s, and N_{ss} for Au/SiO_2/*n*-GaAs SBDs obtained from $I-V$ and capacitance–voltage ($C-V$) characterictics at room temperature and compared with each other.

¶ E-mail: altunhalit@gmail.edu.tr

2. Experimental method

Au/SiO_2/*n*-GaAs SBDs have been prepared using epi-ready *n*-type GaAs wafers with (100) orientations and $(2-3)\cdot 10^{18}\,cm^{-3}$ carrier concentration. For the fabrication process, GaAs wafers were dipped in Ammonium Peroxide for a few seconds to remove native oxide layer on the surface. Au/Ge/Ni ohmic contacts were thermally evaporated to back of the wafers and annealed at 430°C for 40 s. Thin (60 Å) and thick (250 Å) SiO_2 dielectric layers was coated by PECVD technique. SiH_4 gas was used for Si source and O_2 gas used for oxygen source. SBDs with thin and thick SiO_2 insulator layers were named sample 1 and sample 2, respectively. AFM images of $4\,\mu m^2$ scan area were recorded using the needle mode operation on an Omicron VT-STM/AFM system. The root mean square (rms) roughness values were processed from the surface topographies of the samples by Scala Pro software. Circular Au Schottky contacts with 1 mm diameters and 1500 Å thickness were evaporated on both samples in the vacuum system.

The $I-V$ characteristics were perfomed by the use of a Keithly 220 programmable constant current source and Keithley 614 electrometer at room temperature. The $C-V$ measurements were perfomed by using an HP 4192A LF impedance analyzer at 1 MHz and small sinusoidal test signal of 40 mV from the external pulse generator was applied to the samples in order to meet the requirement.

3. Results and discussion

3.1. Surface morphology

AFM is a useful technique for characterizing the surface properties of the thin films. Fig. 1, *a* and *b* shown AFM

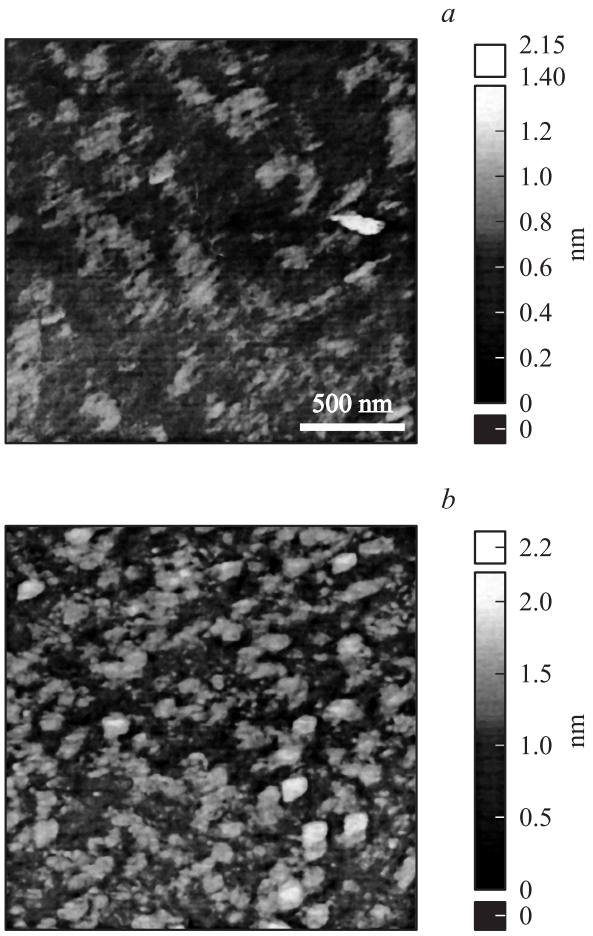

Fig. 1. Surface morphologies of sample 1 (*a*) and sample 2 (*b*) respectively.

images with a $4\,\mu m^2$ scan areas recorded from the SiO_2 cap layer surfaces of sample 1 and sample 2, respectively. For the thickness of 6 nm, there is hardly visible porosity on the surface of sample 1 as can be observed Fig. 1, *a*. Also, sample 1 has a smooth surface with an rms roughness of 0.12 nm. Conversely, for sample 2, there appears a remarkable change in surface morphology of the sample depending on the thickness of the cap layer. As seen in Fig. 1, *b*, the surfaces of the samples 2 displays the grains of varying sizes in the range of 110–140 nm, respectively. This indicates that the lateral sizes of the grains increase as a result of the coalescence of the grains along with increasing cap thickness (6 to 26 nm). Additionally, the grain densities for samples 2 are estimated as $7.5 \cdot 10^8\ cm^{-2}$ by the number of grains from the images. On the other hand, the surface rms roughnesses of sample 2, is measured as 0.25 nm. From the rms values, it is clearly seen that the roughness is closely related to the grain sizes and grain densities on the surfaces of the samples. Table 1 summarizes the thickness, rms roughnesses, grain sizes, and grain densities of the SiO_2 cap layers. As is well known, the mosaicity of the thin films are strongly dependent on lateral sizes of the grains. Wang et al. investigated the effects of grain size on the mosaicity of InN films grown on

Table 1.

Samples	Thickness, nm	*rms*, nm	Grain size, nm	Grain density, cm^{-2}
1	6	0.12	–	–
2	25	0.25	110–140	$7.5 \cdot 10^8$

GaN by MOCVD. They have found that the mosaic twist decreases with increasing grain size and finally approaches to a constant level and the mosaic tilt increases when the grain size becomes large enough [22]. In this context, the high mosaic tilt caused by increment at the grain sizes as a function of cap layer thickness may explain the reason of the rough surfaces for sample 2.

3.2. Analysis of current–voltage (I–V) and capacitance–voltage (C–V) characteristics

Fig. 2 shows the forward and reverse-bias I–V characteristics of Au/SiO_2/*n*-GaAs SBDs at room temperature. When a SBD is considered, it is assumed that thermionic emission current for charge transport under the forward can be expressed as [23].

$$I = I_0 \left[\exp \frac{q}{nkT} (V - IR_s)\right], \qquad (1)$$

where, V is the forward bias voltage, n the ideality factor, and, IR_s the voltage drop across series resistance of the device. The ideality factor n is introduced to calculate the deviation of the experimental I–V date from the ideal thermionic model, and the value of ideality factor should unity for an ideal contact. In Eg. 1, the reverse saturation

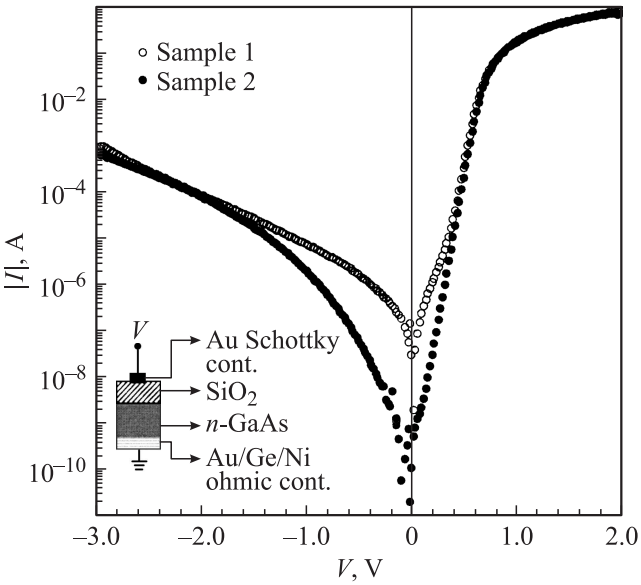

Fig. 2. The semi-logarithmic forward and reverse bias current–voltage characteristics of the Au/SiO_2/*n*-GaAs(MOS) Schottky diodes at room temperatures. Inset figure shows structure of the SBDs.

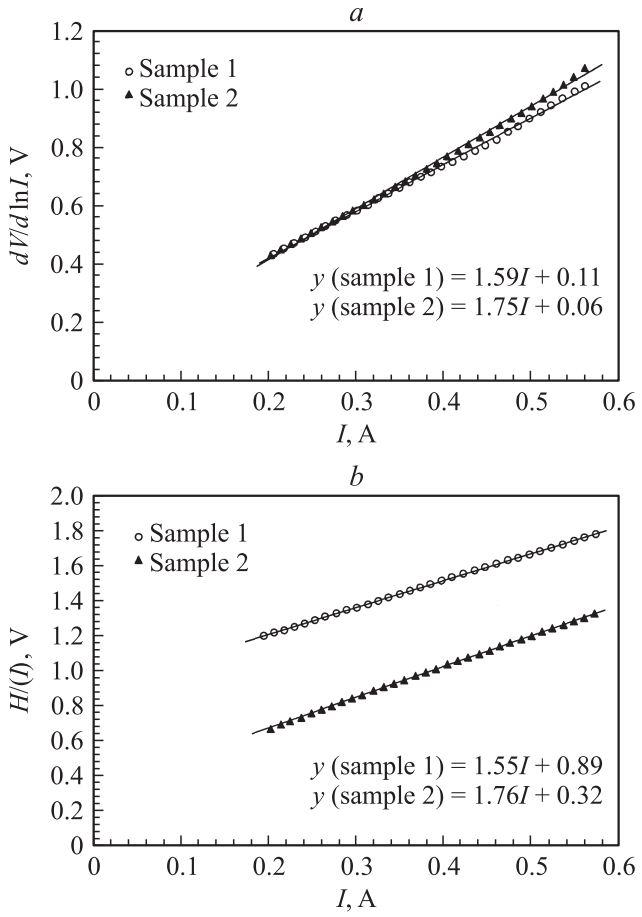

Fig. 3. *a* — experimental $dV/\mathrm{div}(I)$ vs. I and *b* — $H(I)$ vs. I plots for the sample 1 and sample 2.

current I_0 derived from the straight-line intercept of $\ln I$ at zero bias and is given by

$$I_0 = AA^*T^2 \exp \frac{(-q\phi_{B0})}{kT}, \tag{2}$$

where, the quantities A, A^*, q, k, T and ϕ_{B0} are the diode area, the effective Richardson constant and equals to $8.16\,\mathrm{A/(cm^2K^2)}$ for *n*-type GaAs [12], the electronic charge, the Boltzmann constant, temperature in K and the zero-bias barrier height, respectively.

For both samples, in the reverse bias, the „soft“ of slightly non-saturating behavior was observed which may be explained in terms of the image force lowering of Schottky barrier height (SBH) [24,25] and the presence of the interfacial oxide layer between the metal and GaAs wafer.

From Eq.(1), the ideality factor n can be written as

$$n = \frac{q}{kT} \frac{d(V - IR_s)}{d(\ln I)}. \tag{3}$$

The ϕ_{B0} was calculated using theoretical value A^* $(8.16\,\mathrm{A/(cm^2K^2)})$ and extrapolated I_0 at room temperature according to

$$\phi_{B_0} = \frac{kT}{q} \ln \left(\frac{AA^*T^2}{I_0} \right) \tag{4}$$

The experimental values of ideality factors (n) and ϕ_{B0} were calculated as 1.51 and 0.75 eV for sample 1. and 1.33 and 0.75 eV for sample 2, respectively.

Due to the existance of the series resistance (R_s), voltage drop is observes at large forward currents. In this case, the $\ln I = f(V)$ plot deviates from a straight line at high forward. The series resistance is important in the downward curvature of the forward-bias $I-V$ characteristics. Therefore R_s were evaluated using a method developed by Cheung and Cheung [26] in the high-current range where the $\ln I = f(V)$ characteristics are not linear. According to this method from Eq. (1), the folliwing functions can be written

$$\frac{dV}{d \ln I} = n \frac{kT}{q} + IR_s, \tag{5}$$

$$H(I) = V + n \frac{kT}{q} \ln \left(\frac{I}{AA^*T^2} \right) \tag{6}$$

and $H(I)$ is given as

$$H(I) = n\Phi_{b0} + IR_s. \tag{7}$$

Eqs (5) and (7) should give a straight line for the data of downward-curvature region in the forward-bias $I-V$ characteristic. Thus, slopes of $dV/d(\ln I)$ vs I and of $H(I)$ vs. I plots will give R_s. The obtained R_s values from these plots (Fig. 3, *a* and *b*) are given in Table 2.

As can be seen in Table 2, n ideality factor for sample 2 is lower than sample 1. The obtained R_s values by different technique are in good agreement with each other and the R_s value of the Sample 1 has been found the smaller than those sample 2. This behavior can be attributed to the existence of a thick interfacial insulator layer (SiO_2) between Au and GaAs. The effect of the series resistance R_s is usually modeled with a series combination of a diode and a resistor with resistance R_s, through which the current I flows.

The $C-V$ characteristics are one of the fundamental properties of the Schottky barrier diodes. Fig. 4 shows the $C-V$ characteristics at room temperature measured at frequency of 1 MHz by using HP 4192 A Impedance Analyzer (5 Hz–13 MHz) and the test signal of 40 mV. As can be seen in Fig. 4 that while $C-V$ characteristics show that capacitance increases with increasing voltage and the $C-V$ characteristic has an anomalous peak. It is well known that the capacitance of Schottky barrier diode is extremely

Table 2.

Samples	I_a, A	n	$\Phi_{B_0}(I-V)$, eV	$R_s(dV/d \ln I)$, Ω	$R_s(H(I))$, Ω
1	$1.65 \cdot 10^{-9}$	1.51	0.75	1.59	1.55
2	$1.76 \cdot 10^{-10}$	1.33	0.81	1.75	1.76

sensitive to the interface states. In Fig. 4, the zero bias capacitance of sample 1 and sample 2 drop peak values, due to interfacial layer. When a forward bias V is applied across the device, the applied voltage V will be shared by the interfacial layer (V_i), the depletion layer (V_s), and the series resistance combination of the device R_s, and thus V can be written as

$$V = V_s + V_i + IR_s. \tag{8}$$

In addition, when the interfacial layer is sufficiently thick and the transmission probability between the metal and the interface states is very small, the effective barrier height Φ_e is assumed to bias dependent due to presence of an interfacial insulator layer and interface states located between interfacial layer and semiconductor interface, and is given by, [3,27,28]

$$\begin{aligned}\Phi_e &= \Phi_{bo} + \beta(V - IR_s) \\ &= \Phi_{bo} + \left(1 - \frac{1}{n}\right)(V - IR_s).\end{aligned} \tag{9}$$

where β is the voltage coefficient of the effective barrier height Φ_e used in place of the barrier Φ_e [19,29], and for an SBD the ideality factor n becomes greater than unity as proposed by Card and Rhoderick [6],

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V)\right], \tag{10}$$

where W_D is the space charge width, N_{ss} is the density of interface states, $\varepsilon_s = 13.1\varepsilon_0$ and $\varepsilon_i = 4\varepsilon_0$ [12] are the permittivities of the semiconductor and interfacial layer, ε_0 is the permittivity of the free space, and δ is the thickness of the insulator layer. The values of δ and W_D were calculated from capacitance and conductance measurements (1 MHz). The interfacial oxide layer thickness δ was obtained from $C-V$ characteristics using the equation for insulator layer capacitance $(C_{ox} = \varepsilon_i\varepsilon_0 A/\delta)$ where C_{ox} is the oxide capacitance in strong-accumulation region at 1 MHz and A is the diode area [12,17,30]. The values of δ and W_D were found to be about 67 Å and 0.028 μm for sample 1, and 264 Å and 0.063 μm for sample 2, respectively.

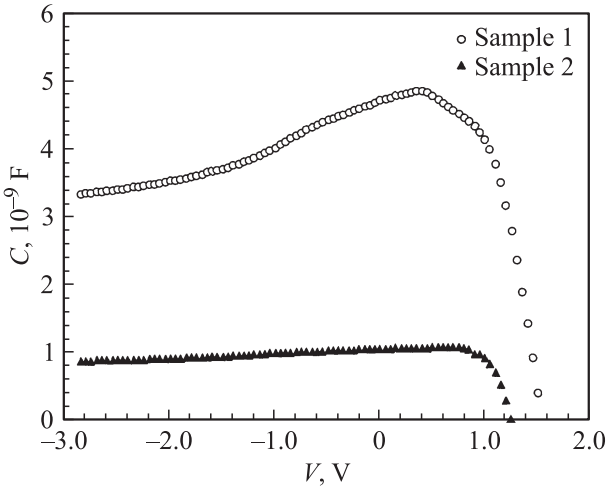

Fig. 4. The experimental capacitance–voltage characteristics of sample 1 and sample 2 at the frequency of 1 MHz at room temperature.

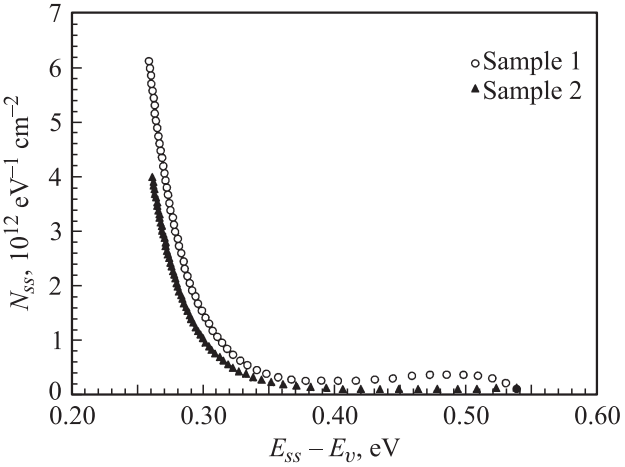

Fig. 5. The interface states energy distribution curves of sample 1 and sample 2 at room temperature.

Furthermore, in n-type semiconductors, the energy of the interface states with respect to the top of the conduction band at the surface of the semiconductor is given by [18,31].

$$E_c - E_{ss} = q(\Phi_e - V). \tag{11}$$

Fig. 5 shows the energy distribution profile of N_{ss} obtained from the forward-bias $I-V$ characteristics of the diodes at room temperature. As can be seen from Fig. 5, the exponential growth of the interface state density from midgap towards the bottom of the conduction band is very apparent, and the interface state density values obtained decrease with applied voltage. This confirms that the density of interface states changes with bias and each of applied biases corresponds to a position inside the GaAs gap. Also, as can be seen in Fig. 5, N_{ss} values for sample 2 are lower than sample 1. Such behavior can be ascribed to the fact that sample 2 has a thicker oxide layer than that of the sample 1 because of which the dangling bonds on the GaAs surface saturate well. In addition, the reduction in the saturation current in the sample 2 for low voltage is caused by the thick SiO_2 layer and is due to a combination of increased barrier height at metal/semiconductor interface and reduced velocity of charge carriers.

4. Conclusion

In this study, thin and thick SiO_2 dielectric layer were deposited on high quality n-type GaAs semiconductor substrate to explain effects of dielectric layer thickness on electrical parameters for Au/SiO_2/n-GaAs SBDs. AFM results show that SiO_2 surface morphology of sample 1

and sample 2 had porosity structure and grain structure, respectively. The ideality factor, leakage current level, and interface state density for sample 2 was found lower than sample 1. The value of R_s has been calculated from high current region of the diodes by using Cheung functions. It's seen that there is a good agreement between the values of the series resistance obtained from two Cheung plots. As a result, we can say that Au/GaAs Schottly barrier diodes have about 25 nm SiO_2 dielectric layer thicknesses shown good diode characteristics.

The authors would like to thank Michael Schneiderman at Submicron Research Center at Weizmann Institute of Science for SiO_2 coating by PECVD. This study was supported by the Turkish Prime Ministry state Planning Agency under project no: 2001K120590 and The European Transnational Access Program #RITA-CT-2003-506095 WISSMC.

References

[1] R. Hackam, P. Harrop. IEEE Trans. Electron. Dev., **19**, 1231 (1972).
[2] S. Ashok, J.M. Borrego, R.J. Gutmann. Sol. St. Electron., **22**, 621 (1972)
[3] S. Altindal, I. Dokme, M.M. Bülbül, N. Yalçin, T. Serin. Microelectron. Eng., **83**, 499 (2006).
[4] A. Singh, K.C. Reinhhardt, W.A. Anderson. J. Appl. Phys., **68** (7), 3475 (1990).
[5] P. Chattopadhyay, A.N. Daw. Sol. St. Electron., **29** 555 (1986).
[6] H.C. Card, E.H. Rhoderick. J. Phys. D: Appl. Phys., **4** 1589 (1971).
[7] K. Hatori, Y. Toru. Sol. St. Electron., **34**, 531 (1991).
[8] M. Biber. Physica B, **325**, 138 (2003).
[9] B. Akkal, Z. Benamara, L. Bideux, B. Gruzza. Microelectron. J., **30**, 673 (1999).
[10] P. Cova, A. Singh. Sol. St. Electron. **33**, 11 (1990).
[11] C.H. Liu, T.K. Lin, S.J. Chang. Sol. St. Electron., **49**, 1077 (2005).
[12] S.M. Sze. *Physics of Semiconductor Devices*, second edn (Wiley, N.Y., 1981).
[13] A.K. Ghosh, T. Feng, J.I. Haberman, H.P. Maruska. J. Appl. Phys., **55**, 2990 (1984).
[14] A.K. Ghosh, C. Fishman, T. Feng, K.K. Ng, H.C. Card. J. Appl. Phys., **51**, 2153 (1980).
[15] Í. Dökme. Physica B, **388**, 10 (2007).
[16] A. Singh, K.C. Reinhhardt, W.A. Anderson. J. Appl. Phys., **68** (7) 3475 (1990).
[17] Ş. Altindal, S. Karadeniz, N. Tuğluoğlu, A. Tataroğlu. Sol. St. Electron., **47** 1847, (2003).
[18] M.K. Hudait, S.B. Kruppanidhi. Sol. St. Electron., **44**, 1089 (2000).
[19] H. Çetin, E. Ayyildiz. Appl. Surf. Sci., **253**, 596 (2007).
[20] H. Altuntas, S. Altindal, S. Özcelik, H. Shtrikman. Vaccum, **83**, 1065 (2009).
[21] H. Altuntas, S. Altindal, H. Shtrikman, S. Özcelik. Microelectron, Reliab., **49**, 904 (2009).
[22] H. Wang, Y. Huang, Q. Sun, J. Chen, L.L. Wang, J.J. Zhu, D.G. Xhao, S.M. Zhang, D.S. Jiang, Y.T. Wang, H. Yang. Appl. Phys. Lett., **89**, 092 114 (2006).
[23] E.H. Rhoderick, R.H. Williams. *Metal-Semiconductor Contacts*, second edn (Clarendon Press, Oxford, 1988).
[24] T.U. Kampen, S. Park, D.R.T. Zahn. Appl. Surf. Sci., **190**, 461 (2002).
[25] A. Bolognesi, A.Di. Carlo, P. Lugli, T. Kampen, D.R.T. Zahn. J. Phys.: Condens. Matter, **15**, 2719 (2003).
[26] S.K. Cheung, N.W. Cheung. Appl. Phys. Lett., **49**, 85 (1986).
[27] J.H. Werner, H.H. Guttler. J. Appl. Phys., **69**, 1522 (1991).
[28] J. Osvald, Z.J. Horvarth. Appl. Surf. Sci., **234**, 349 (2004).
[29] Ş. Karatas, Ş. Altindal. Mater. Sci. Eng. B, **122**, 133 (2005).
[30] E.H. Nicollian, A. Goetzberger. Appl. Phys. Lett., 7216 (1965).
[31] E.H. Nicollian, J.R. Brews, *MOS Physics and Technology* (John Wiley and Sons, N. Y., 1982).

Редактор Т.А. Полянская