Comparative investigation of InP/InGaAs abrupt, setback, and heterostructure-emitter heterojunction bipolar transistors

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In this paper, the characteristics of InP/InGaAs abrupt, setback, and heterostructure-emitter heterojunction bipolar transistors (HBTs) are comparatively investigated by twodimensional simulation analysis. In the setback (heterostructure-emitter) HBT, a thin 50 Å undoped $In_{0.53}Ga_{0.47}As$ (n-$In_{0.53}Ga_{0.47}As$) layer is inserted between n-InP emitter and p^+-InGaAs base layers to lower the energy band at emitter side for decreasing the collector-emitter offset voltage. The simulated results exhibits that the abrupt HBT has the largest current gain, the largest collector-emitter offset voltage, and the smallest unity gain cutoff frequency. While, the setback and heterostructure-emitter HBTs exhibit the smallest current gain and offcet voltage, respectively. Consequentially, the demonstration and comparison of the three-type HBTs provide a promise for design in circuit applications.

1. Introduction

Over the past years, InP-based heterojunction bipolar transistors (HBTs) have been widely used for optical communications, low $1/f$ noise, high frequency, and signal amplification applications [1–3]. As compared to the GaAs-based HBTs, the major advantages of InP/InGaAs HBTs include

(i) the lower surface recombination velocity on base layer,

(ii) the lower base-emitter turn-on voltage,

(iii) the lower electron effective mass and higher electron mobility in InGaAs material layer,

(iv) the higher etching selectivity between InP and InGaAs material layers.

Though a considerable valence band discontinuity (ΔE_V) of 0.35 eV at InP/$In_{0.53}Ga_{0.47}As$ heterojunction could provide good confnement effect for holes, a large conduction band discontinuity (ΔE_c) of 0.25 eV is still a significant factor to result in large collector-emitter (C-E) offset voltage (ΔV_{CE}), which increases unnecessary power consumption in circuit applications [4,5].

Several improved devices, such as setback HBTs, heterostructure-emitter bipolar transistors (HEBTs), and double HBTs (DHBTs), etc., have been demonstrated to reduce the offset voltages and maintain current gains [5–10]. Regarding to the setback HBTs, by inserting a thin as well as undoped layer between emitter and base region could lower the barrier height at emitter side, reduce the potential spike and turn-on voltage at base-emitter (B-E) junction, and prevent base dopant out-diffusion, simultaneously [5]. However, it will form spacer region recombination current and degrade the device performance. With respect to the HEBTs, the offset voltage could be also reduced for the decrease of potential spike at B-E junction by the employment of a small energy-gap material layer between the emitter and base layers. In addition, the large energy-gap emitter layer can keep a good confinement effect for holes injecting from the base into the emitter, and maintain a high current gain [6–8]. Nevertheless, if the small energy-gap material layer is too thick, the transistor will act with inferior confinement effect for holes. Then, the charge storage in neutral-emitter region will enhance the base recombination current, increase the base current, and degrade the current gain, simultaneously [6]. For the DHBTs with a large energy-gap collector layer, the symmetric structures of B-E and B-C junctions enable the difference of B-E and B-C turn-on voltages to decrease, and then the offset voltage is substantially improved [9,10]. But, the injecting electrons will be blocked at base-collector heterojunction under transistor operation. In general, the DHBTs show smaller collector current and gain than the conventional HBTs.

The individual HBT possesses different characteristics though most of HBTs have the similar structure layers. However, some material layers in HBTs are critical and device characteristics are significantly affected by the epitaxial condition, process and reliability. The simulated analysis will be proper to demonstrate and compare the device performance difference each other. In this article, the device characteristics, including collector current, current gain, C-E offset voltage, electron and hole distributions, and unity current cutoff frequency, of the InP/InGaAs HBTs with abrupt, setback, and heterostructure-emitter structures will be compressively studied. To our knowledge, there is not any paper corresponding to the comparison of the three-type devices is reported until now.

2. Device structures

The studied devices were constructed on semiinsulating GaAs substrates. In the conventional InP/InGaAs abrupt HBT, labeled device A, the structure layers consist of 0.5 μm, $n^+ = 10^{19}\,cm^{-3}$ $In_{0.53}Ga_{0.47}As$ subcollector layer; 0.5 μm, $n^- = 5 \cdot 10^{16}\,cm^{-3}$ $In_{0.53}Ga_{0.47}As$ collector layer; 1000 Å, $p^+ = 10^{19}\,cm^{-3}$ $In_{0.53}Ga_{0.47}As$ base layer; 1000 Å, $n = 5 \cdot 10^{17}\,cm^{-3}$ InP emitter layer, and 0.3 μm, $n^+ = 10^{19}\,cm^{-3}$ InGaAs cap layer.

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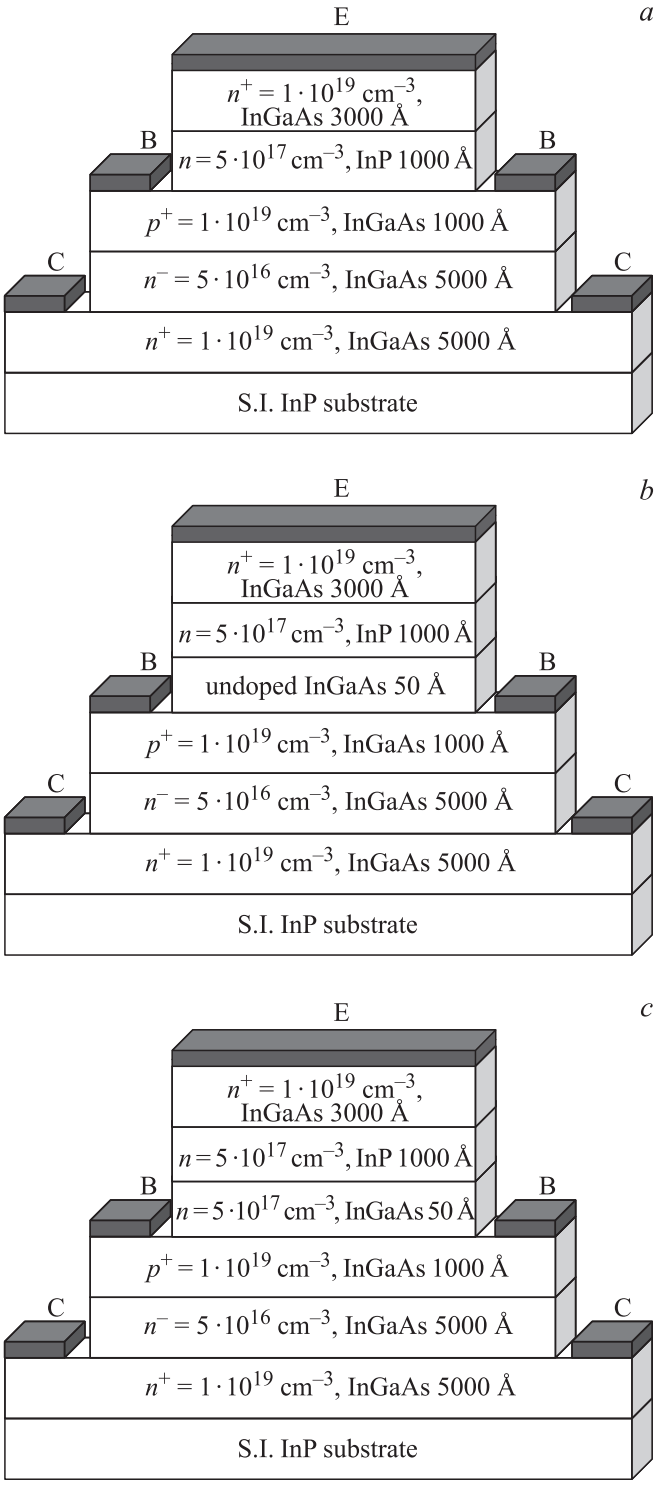

Figure 1. Schematic cross sections of the InP/InGaAs HBTs with (a) abrupt InP emitter layer,(b) i-InGaAs setback layer, and (c) n-InGaAs layer at base-emitter junction.

Similar to the above device structure, a thin 50 Å undoped $In_{0.53}Ga_{0.47}As$ ($n = 5 \cdot 10^{17}$ cm^{-3}) layer was added between n-InP emitter and p^+-InGaAs base layers in the setback and heterostructure-emitter HBTs, which are labeled as devices B and C, respectively. In the three devices, the emitter and collector areas are 50×50 and $100 \times 100\,\mu$m^2 respectively. Figs 1, a, b and c illustrate the schematic cross sections of the abrupt, setback and heterostructure-emitter InP/InGaAs HBTs, respectively. A twodimensional semiconductor simulation package SILVACO was employed to analyze the energy-band diagrams, carrier distributions, dc and high-frequency performance [11]. The simulated analysis takes into account the Poisson equation, continuity equation of electrons and holes, Shockley–Read–Hall (SRH) recombination, Auger recombination, and Boltzmann statistics, simultaneously.

3. Results and discussion

The corresponding energy band diagrams at equilibrium of the devices A, B, and C are revealed in Figs 2, a, b, and c, respectively. Obviously, the devices A exists a considerable potential spike of 0.162 V at B-E junction, while relatively small potential spikes of only 0.02 and 0.006 V are observed for the device B and C, respectively. The potential spike at B-E junction is defined as the difference between the potential peaks at emitter and that at bulk base. Clearly, the employment of a thin undoped (or n-type InGaAs) layer between emitter and base layers will enable the pn junction as a homojunction, and it will lower the energy band at emitter side to reduce the potential spike.

The common-emitter current-voltage characteristics (I–V) of the devices A, B, and C are shown in Figs 3, a, b, and c, respectively. As seen in the figure, the device A exhibits a largest collector current of 152 mA and the device C has the smallest collector current of only 68 mA. Figs 4 , a, b, and c depict the enlarged views of the common-emitter I–V curves of the devices A, B, and C, respectively. The C-E offset voltages of 109.8, 54.8, and 53.5 mV at $I_B = 20\,\mu$A are observed in the devices A, B, and C, respectively. In general, the offset voltages of HBTs mainly result from the difference of turn-on voltages between B-E heterostructure and B-C homojunction. In the device A, a considerable potential spike at B-E heterostructure will cause a large turn-on voltage at B-E junction and result in a large C-E offset voltage. Nevertheless, smaller offset voltages are achieved in the devices B and C, which can be attributed that (i) the energy band at emitter side is substantially lowered to reduce the B-E turn-on voltage by the insertion of an $In_{0.53}Ga_{0.47}As$ layer between emitter and base layers, and (ii) the B-E and B-C junctions are nearly symmetric heterostructures. In addition, as compared to the device B with an InGaAs undoped layer at B-E junction, the device C exhibits a smaller C-E offset voltage because the n-InGaAs layer could effectively reduce potential spike.

The Gummel plots at $V_{BC} = 0$ V are illustrated in Fig. 5. Maximum current gains of 705, 328, and 341 are obtained in the devices A, B, and C, respectively. The B-E turn-on voltage of device A is of 0.445 V at the collector current level of 1 μA, which is greater than that of 0.391 and 0.388 V in the devices B and C, respectively. The low turn-on

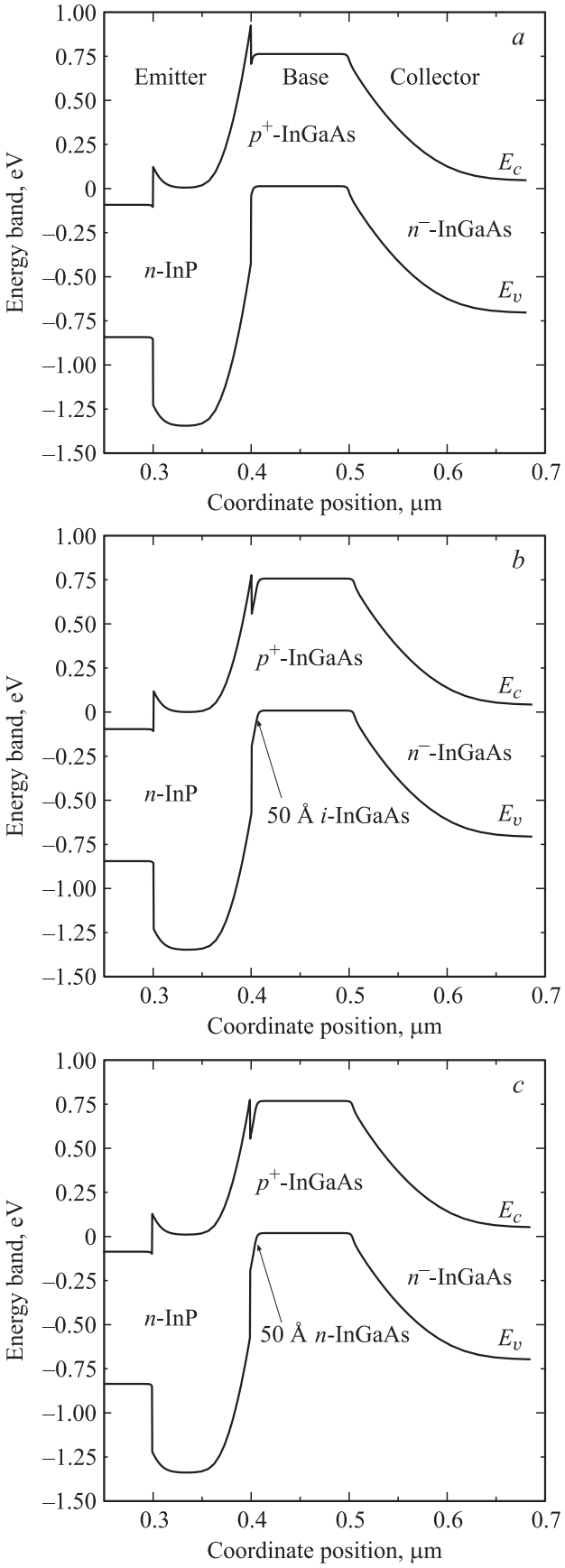

Figure 2. Corresponding energy band diagrams at equilibrium of (*a*) device A, (*b*) device B, and (*c*) device C.

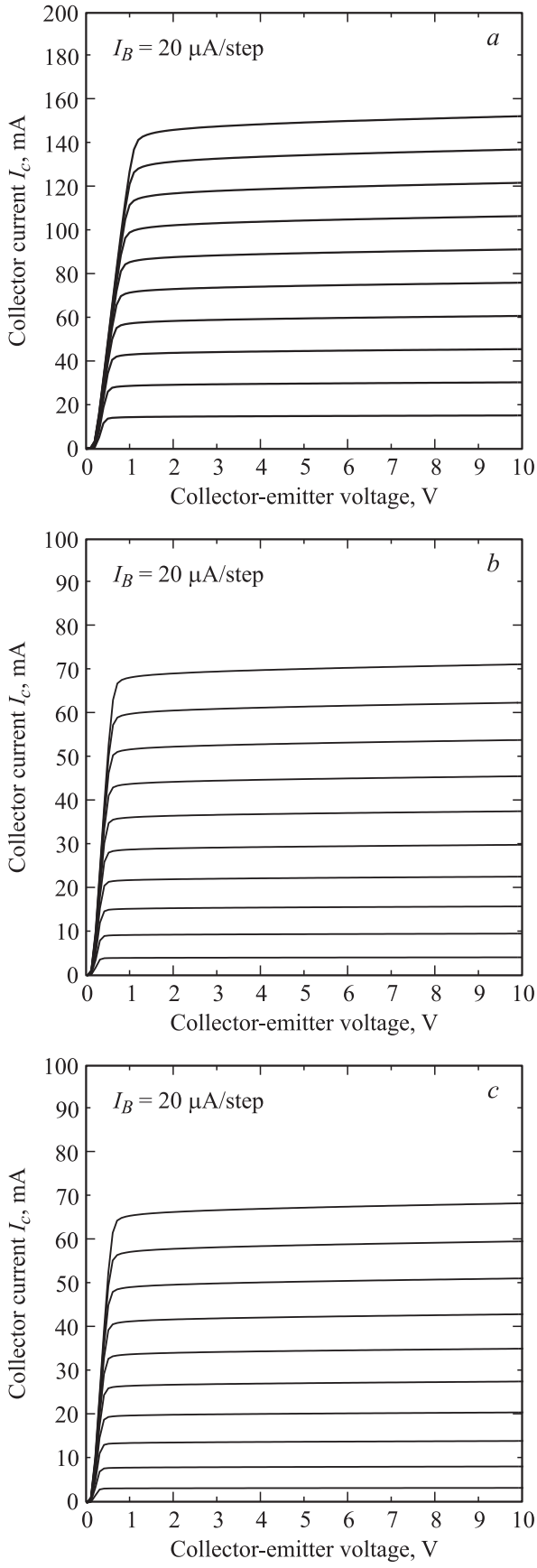

Figure 3. Common-emitter current-voltage characteristics of (*a*) device A, (*b*) device B, and (*c*) device C.

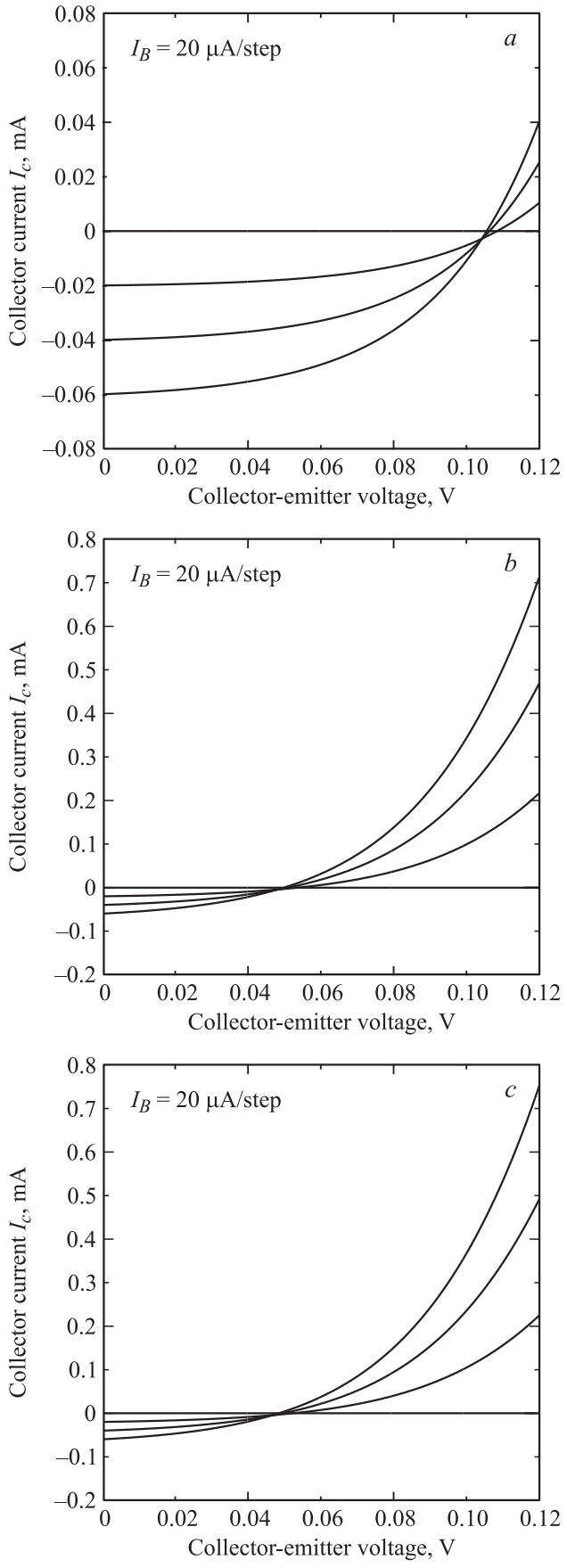

Figure 4. Enlarged view near the origin of the current-voltage characteristics of (*a*) device A, (*b*) device B, and (*c*) device C.

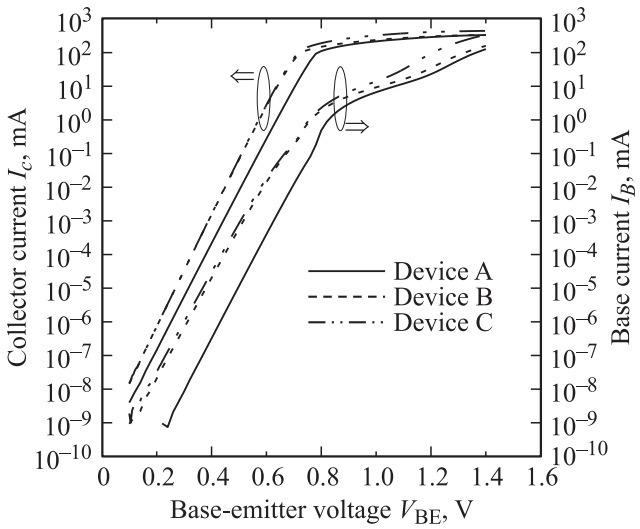

Figure 5. Measured Gummel plots at $V_{BC} = 0$ V of device A, device B and device C.

voltage can reduce *C-E* offset voltage for decreasing the power consumption in circuit applications. As depicted in the figure, at low current levels the ideality factors n_c of collector currents are of 1.079, 1.039, and 1.0 for the devices A, B, and C, respectively. The n_c nearly equal to unity denotes that diffusion mechanism dominates the electron transportation across the *B-E* junction. Nevertheless, the device C has a smallest n_c value due to the neglect of potential spike for the employment of an *n*-type InGaAs layer at *B-E* junction. On the other hand, at low current levels the ideality factor n_b of base currents are of 1.084, 1.178, and 1.22 for the devices A, B, and C, respectively, which means that diffusion mechanism is still significant to dominate the base current. Among of the three devices, the base recombination is the largest value in the device C. These phenomena will be explained in follows.

Figs 6, *a*, *b*, and *c* show the carrier distributions near *B-E* junction at $V_{BE} = 0.7$ V for the devices A, B, and C, respectively. Apparently, there are considerable electron and hole concentrations existed within the *i*-InGaAs (*n*-InGaAs) region in the devices B and C, respectively. That is to say, even though most of holes injecting form base to emitter can be blocked back by the valence band discontinuity at InP/InGaAs heterojunction under transistor operation mod, part of holes are stored within the *i*-InGaAs (*n*-InGaAs) layer and some electrons with the holes may be trapped within the region. Thus, spacer (neutral-emitter) recombination will be formed in the thin spacer (*n*-InGaAs) layer and it causes base current to increase in the device B (device C). So, the current gains of devices B and C are less than the device A with abrupt *B-E* junction. Furthermore, it is worthy to note that due to the *n*-type doping the electron concentration within the *n*-InGaAs layer in the device C is greater than that within the *i*-InGaAs layer in the device B. Consequently, the device C has slightly higher recombination and lower current gain than the device B.

The relationship between current gain and operating frequency of the devices A, B, and C, is depicted in Fig. 7. The unity gain cutoff frequencies f_T are of 14.5, 18.5, and 18.4 GHz in the devices A, B, and C, respectively. In the device A, the f_T value is the smallest of the three devices, which can be attributed that the considerable potential spike enables the transporting time of electrons across the *B-E* junction to increase. In addition, because the electron-hole recombination in the 50 Å *n*-InGaAs layer is slightly higher than that in the 50 Å *i*-InGaAs layer, the device C exhibits a slightly lower f_T value as compared to the device B.

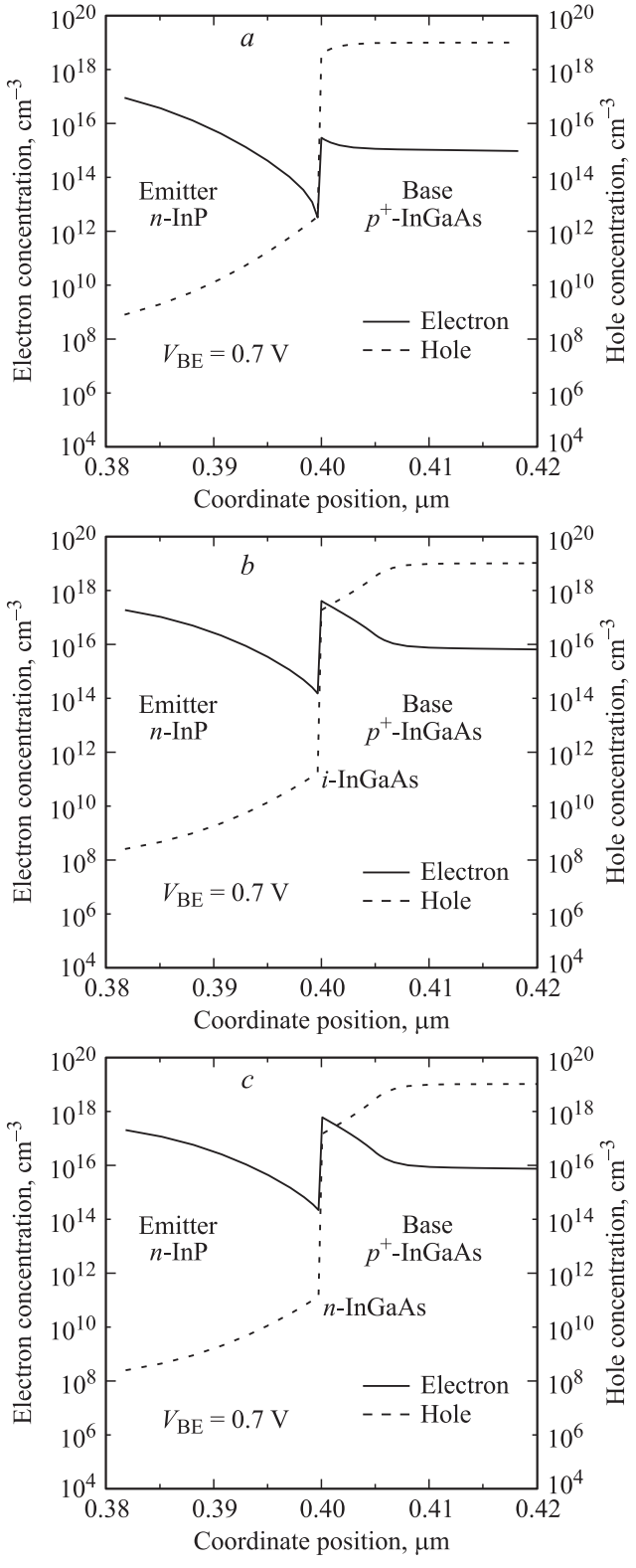

Figure 6. Electron and hole distributions near *B-E* junction at $V_{BE} = 0.7$ V of (*a*) device A, (*b*) device B, and (*c*) device C.

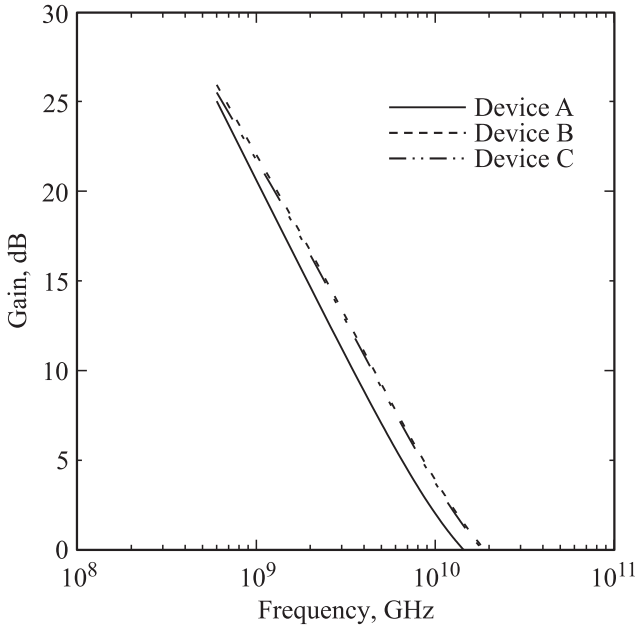

Figure 7. The relationship between current gain and operating frequency of device A, device B and device C.

4. Conclusion

In summary, the characteristics and device mechanisms of InP/InGaAs abrupt, setback, and heterostructure-emitter HBTs have been compressively demonstrated. Due to the insertion of a small energy-gap *i*-InGaAs (*n*-InGaAs) layer between InP emitter and p^+-InGaAs base layers, the potential spike at *B-E* junction and *C-E* offset voltage could be effectively reduced. For comparison, the abrupt HBT exhibits largest collector current, current gain, offset voltage, and a smallest unity gain cutoff frequency. While, heterostructure-emitter HBT shows the smallest *C-E* offset voltage due to the smallest potential spike at *B-E* junction. However, the collector current and gain are the smallest values in the three devices, which could be attributed to the neutral-emitter recombination within the *n*-InGaAs layer at *B-E* junction. In addition, higher unity gain cutoff frequencies of the setback and heterostructure-emitter HBTs are achieved because the injecting electrons can easily transport across the *B-E* junction. Consequently, the comparative study of the studied devices provides a design criterion for signal amplifier and circuit applications.

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